

FIG. 1

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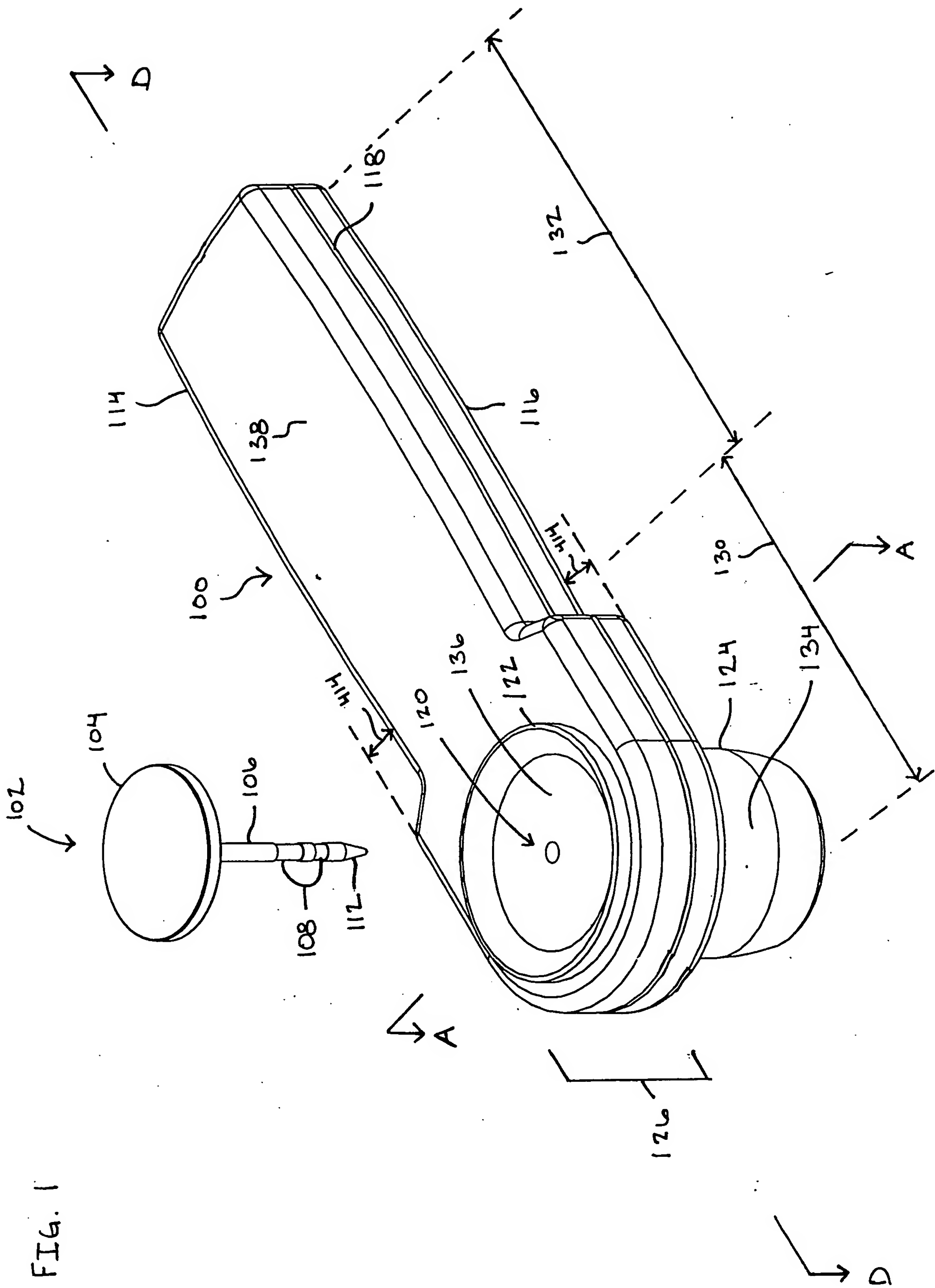


FIG. 2

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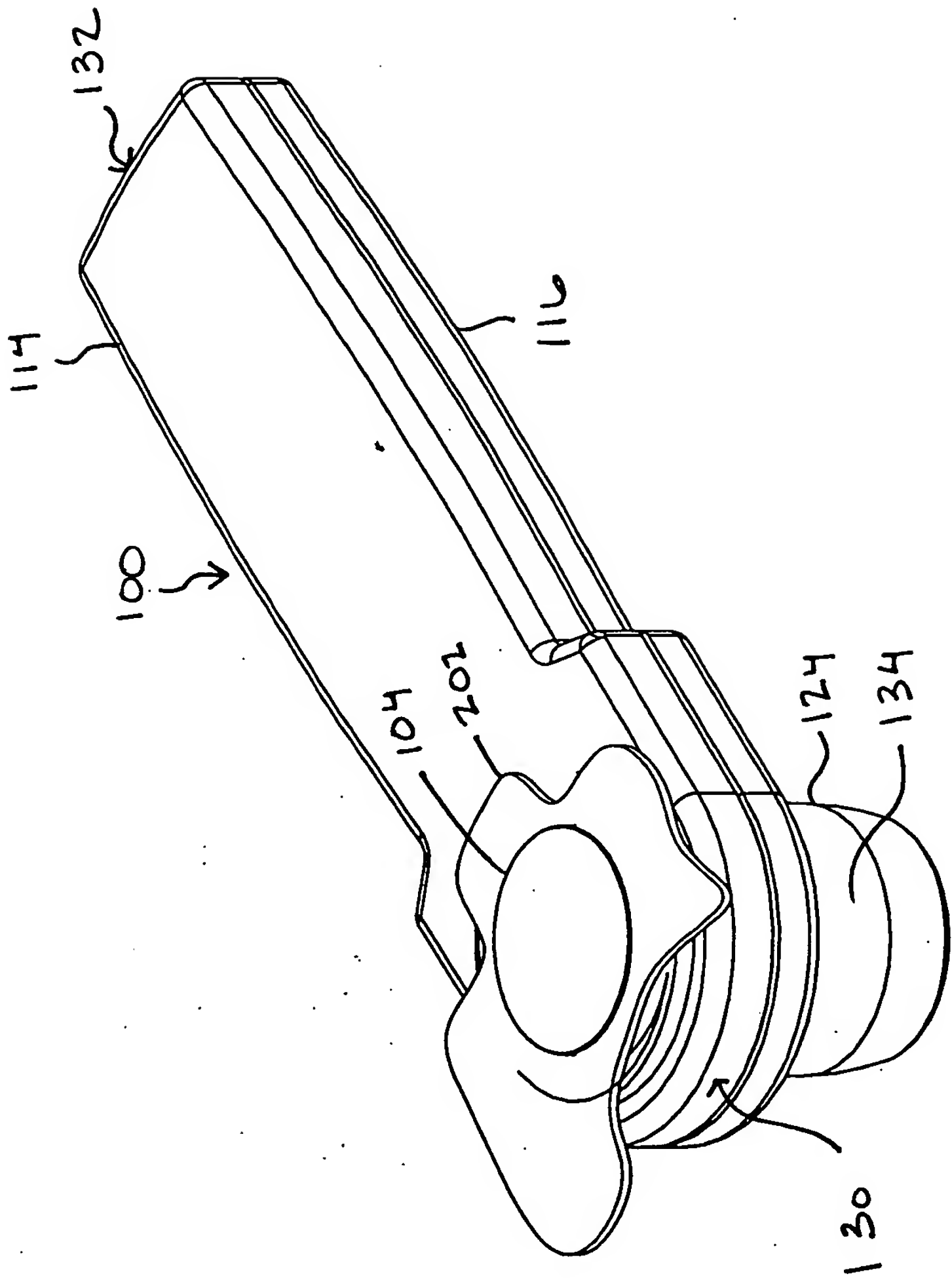


FIG. 3

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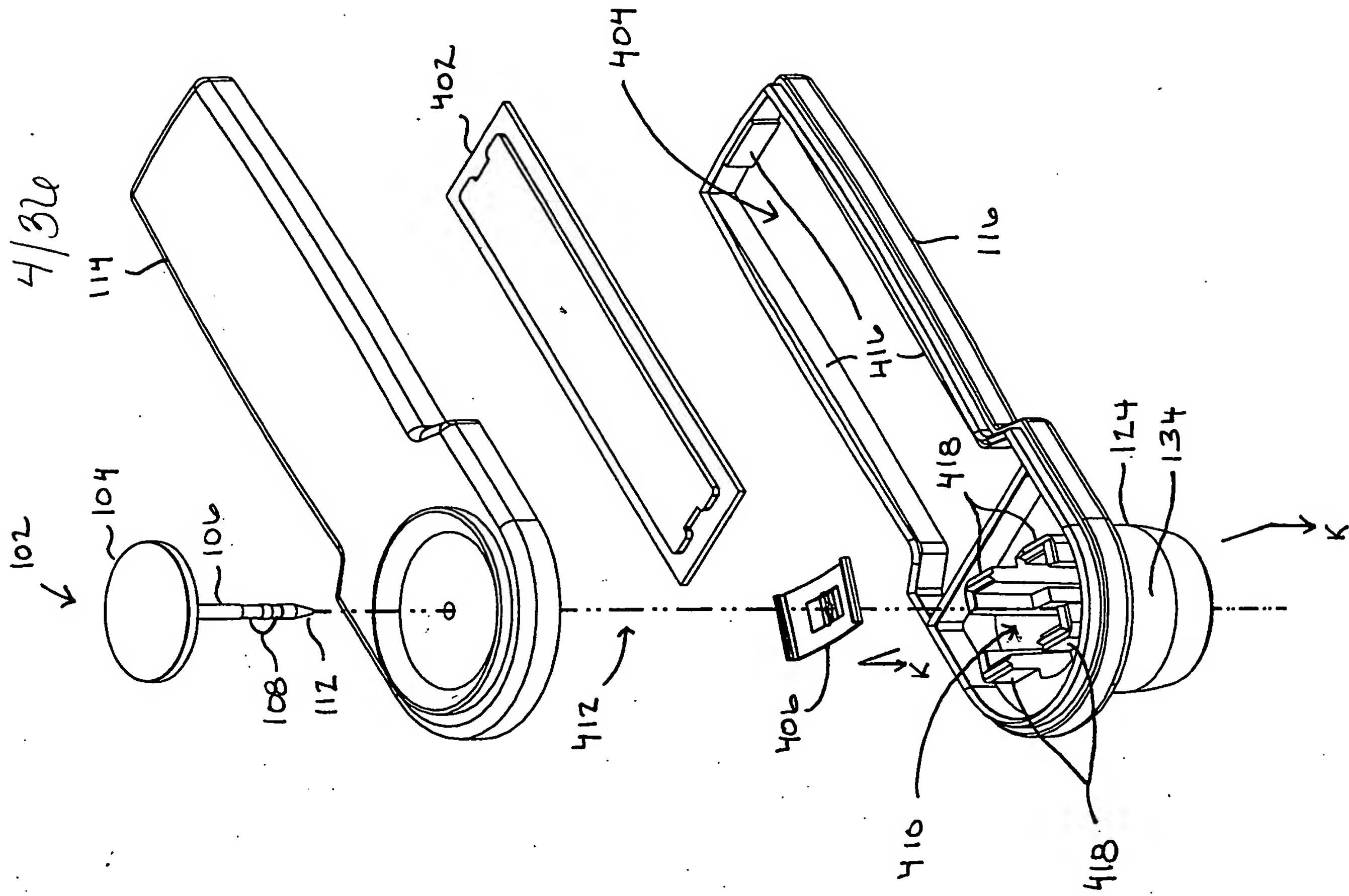


Fig. 4.

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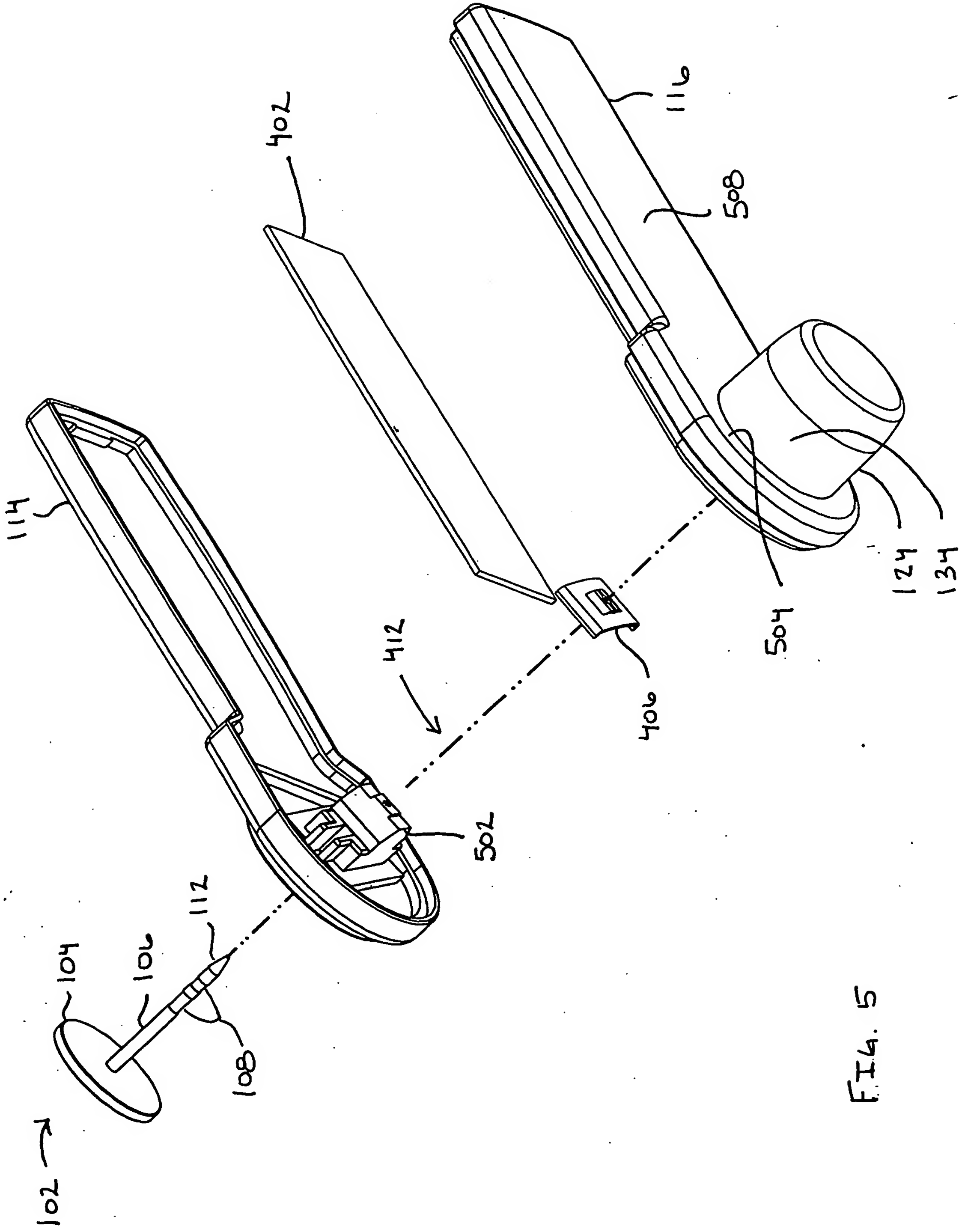


FIG. 5

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602

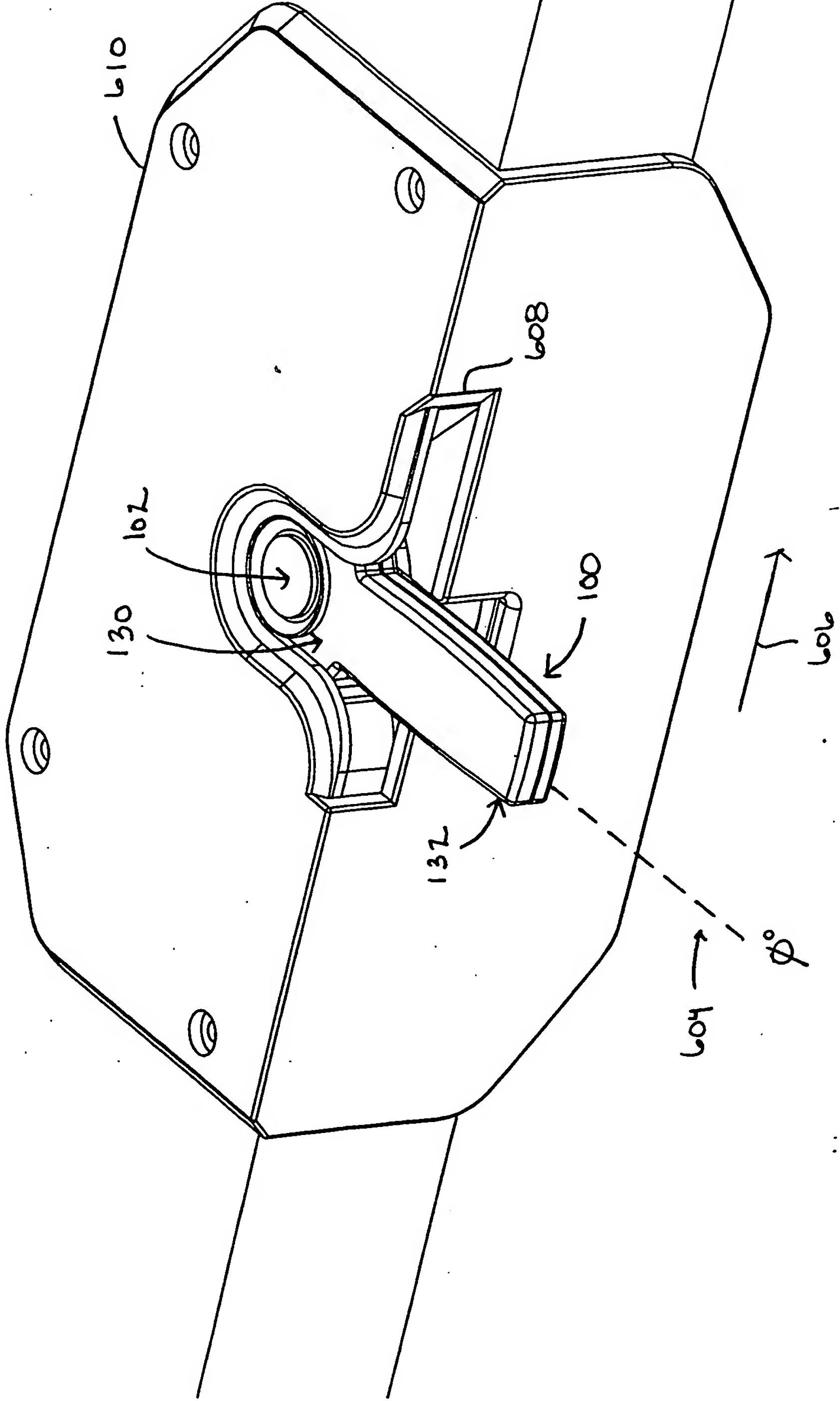


FIG. 6

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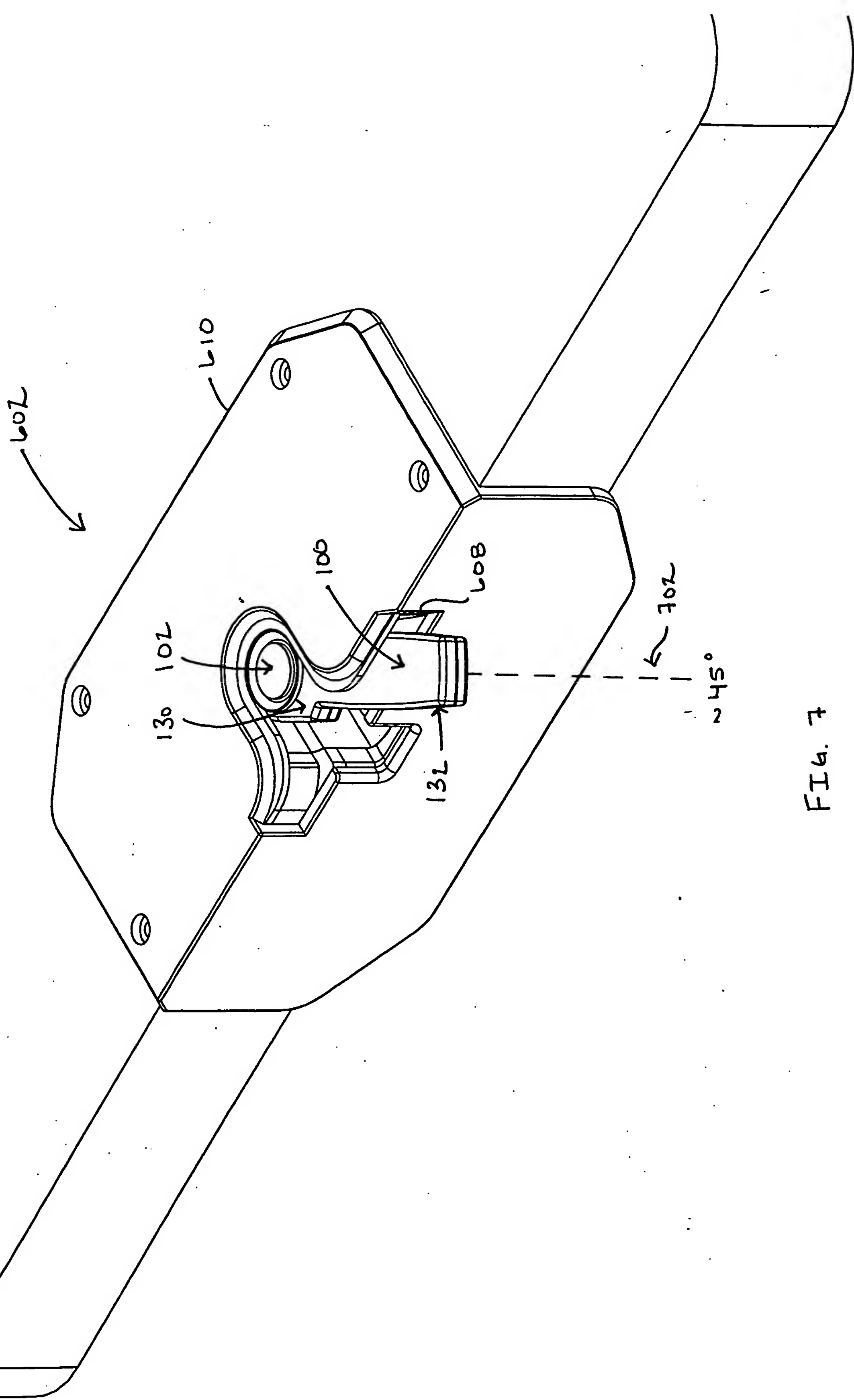


FIG. 7

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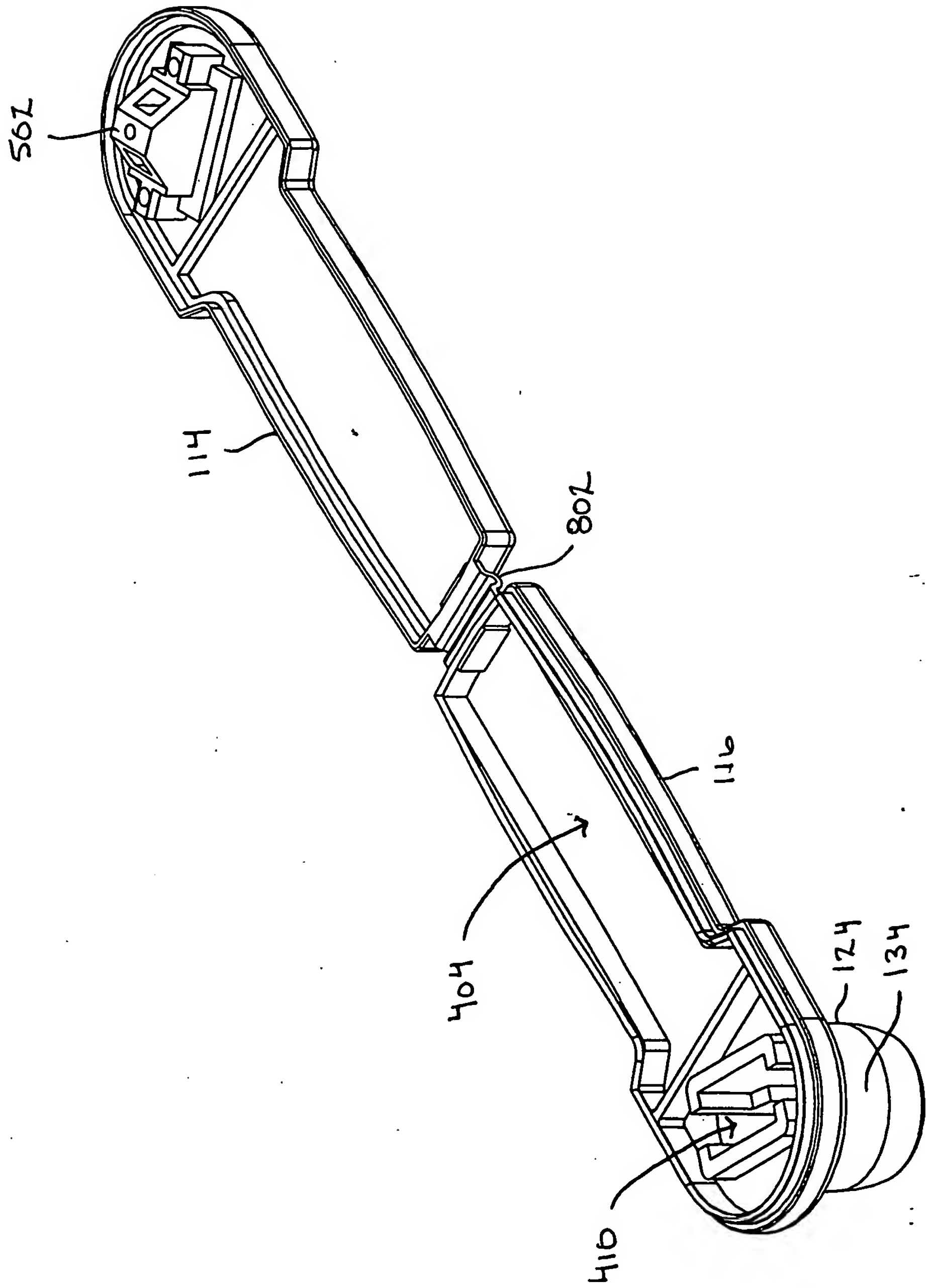


FIG. 8

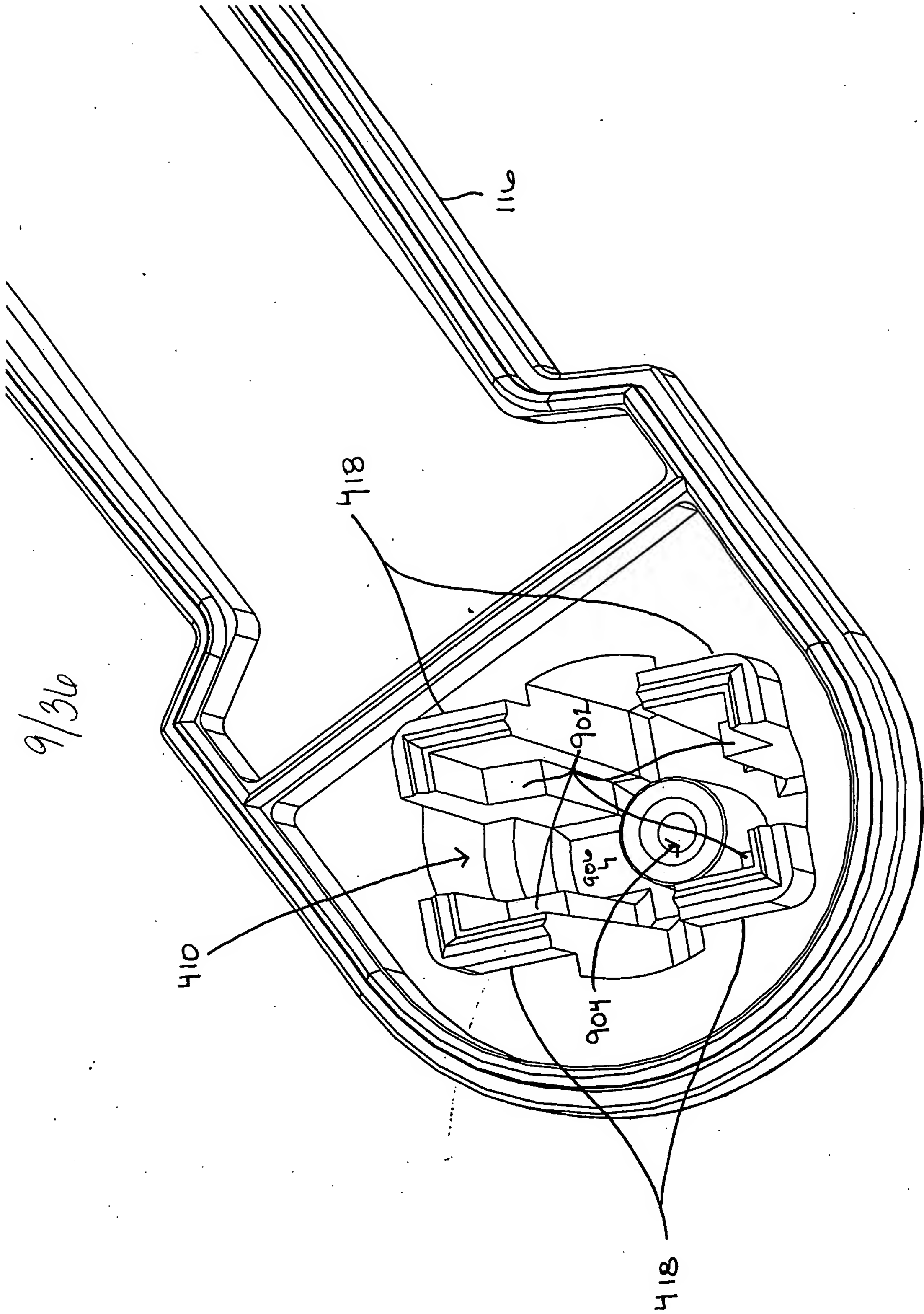


FIG. 9

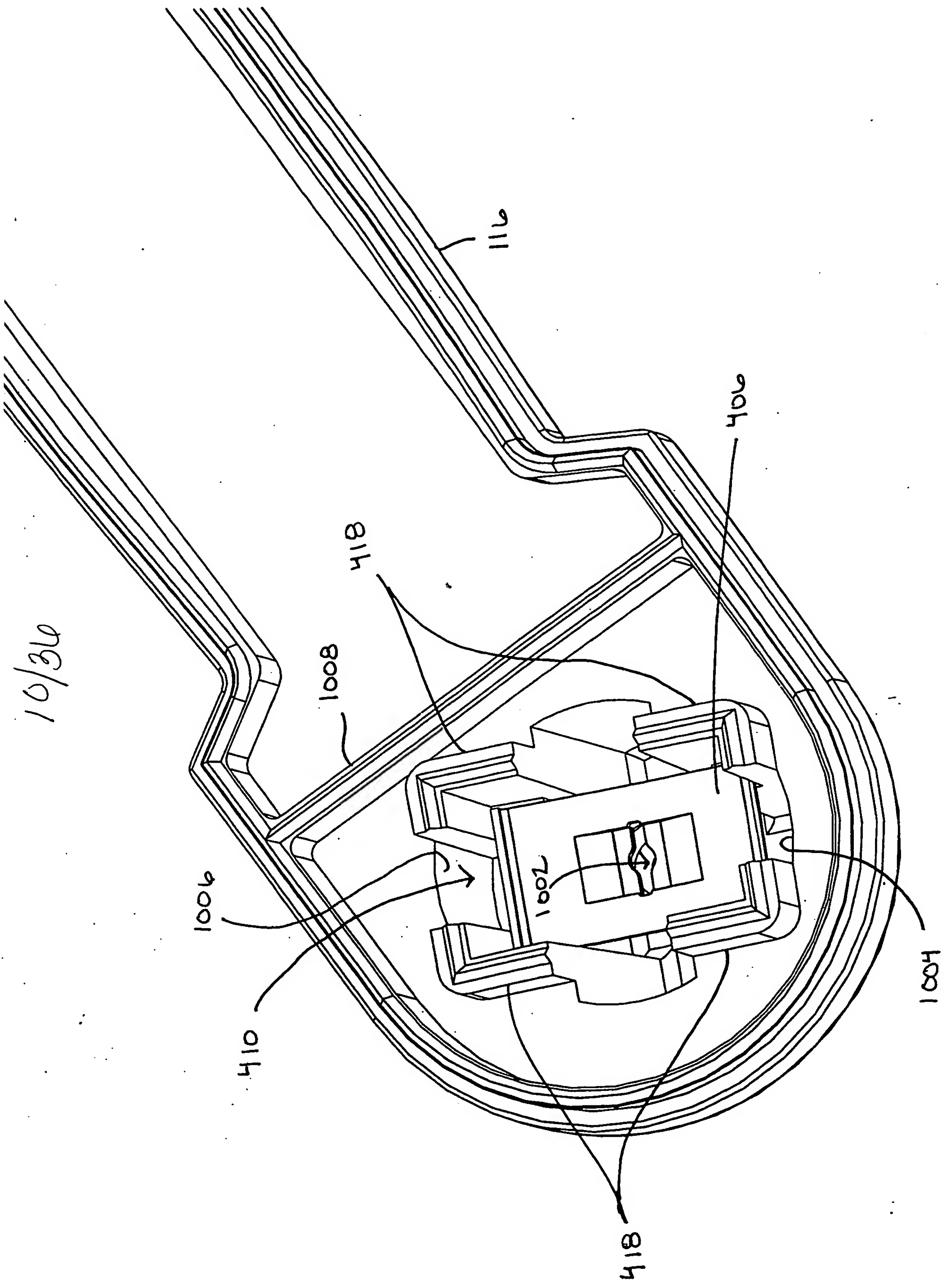


FIG. 10

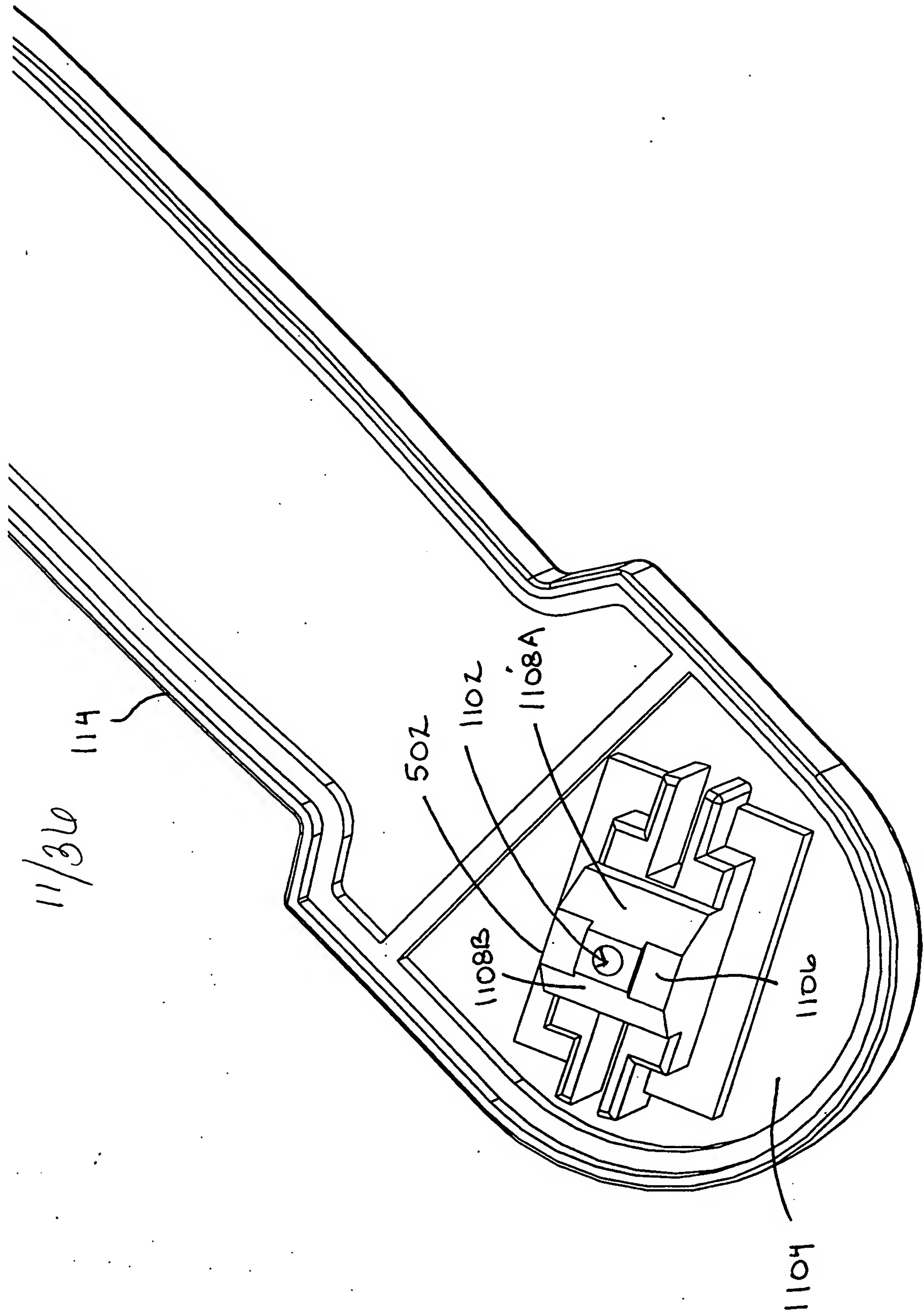


FIG. 11

1200

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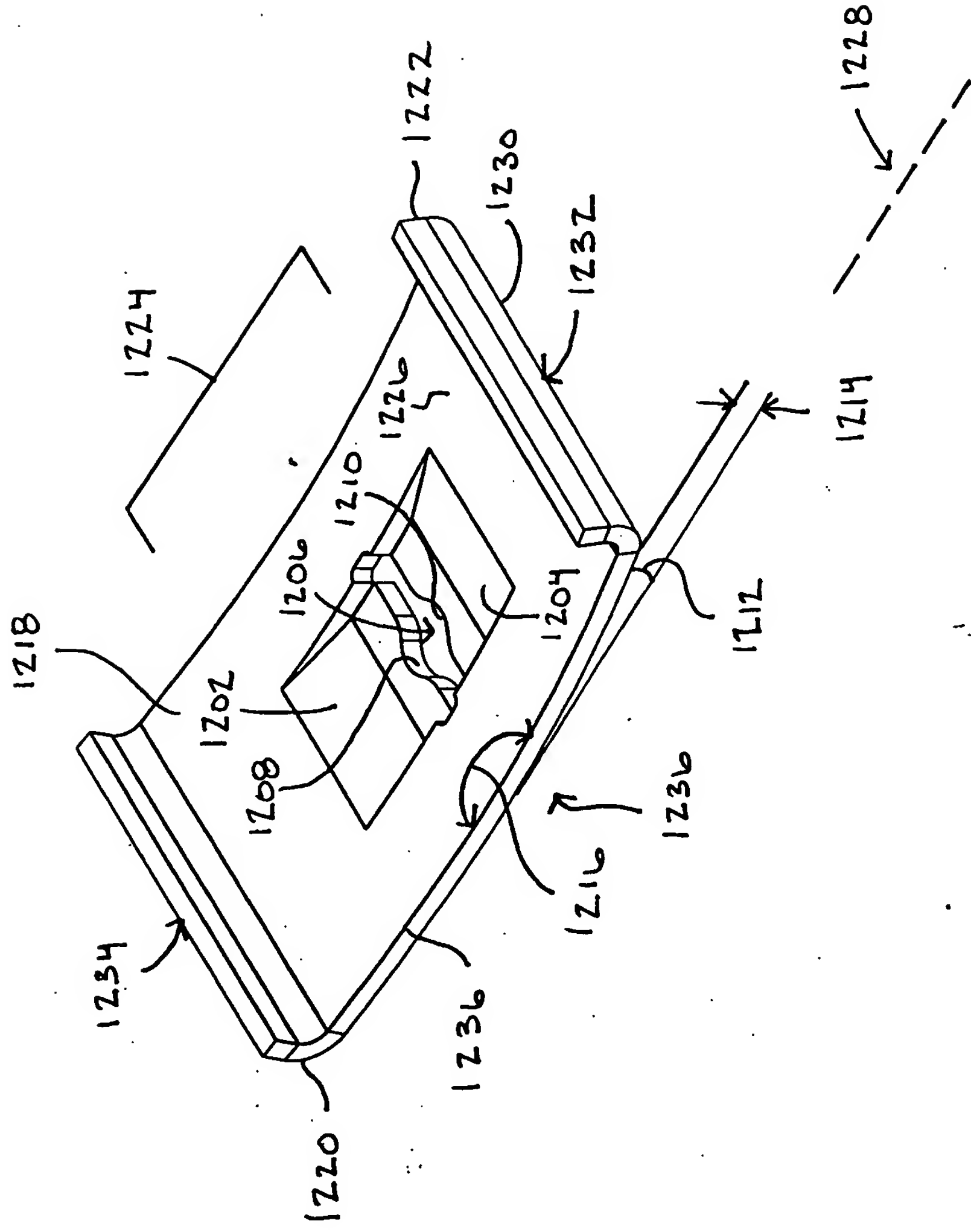


FIG. 12

This cross-sectional view shows a central channel region 120 flanked by side gate regions 100A and 100B. The channel is defined by a central layer 122 and side layers 124. The side gates are formed by a gate stack 110 and a gate electrode 130. The channel is surrounded by a gate dielectric 100C. The device is shown in a cross-section along a dashed line 130A.

Fig. 13

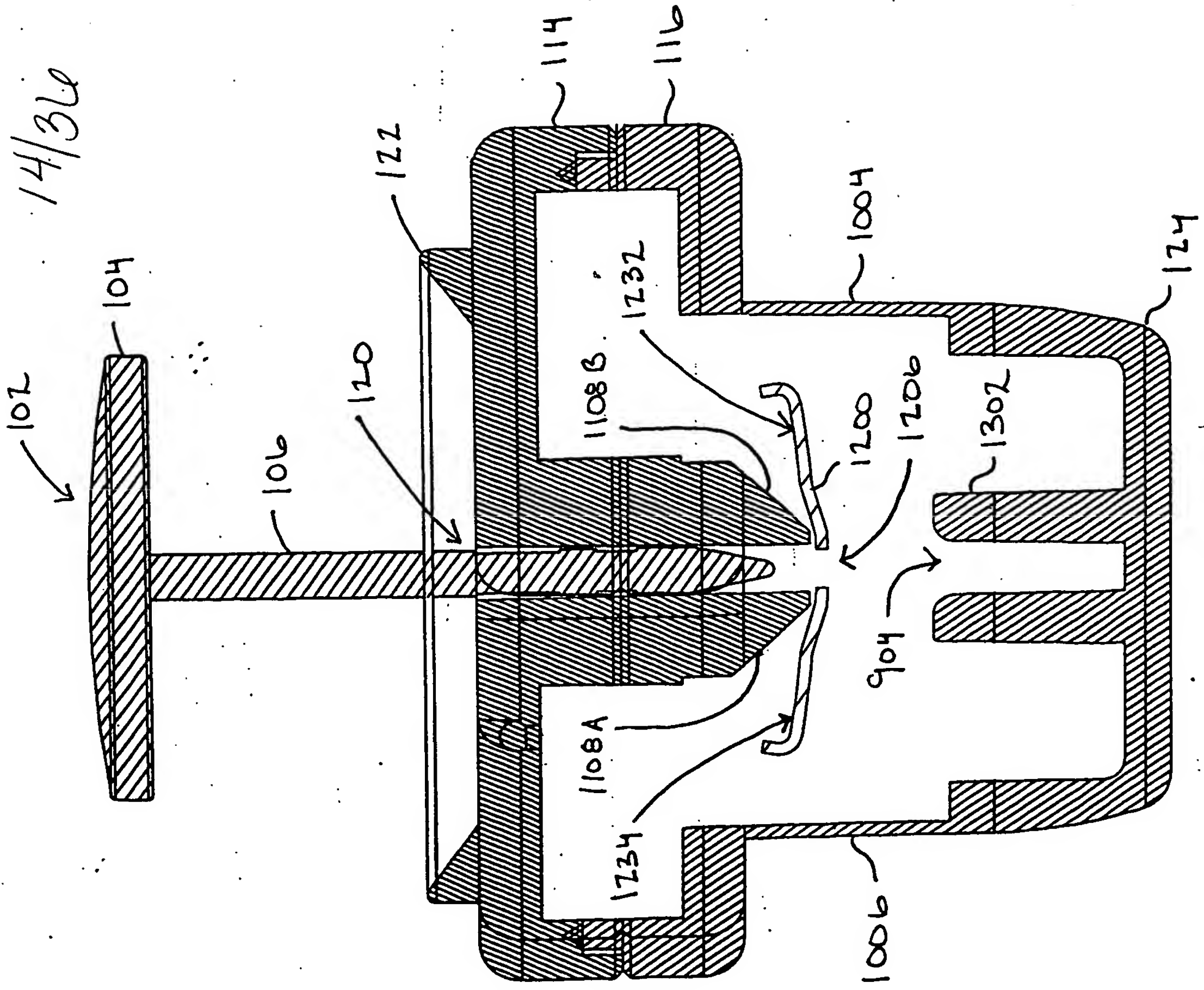


FIG. 14

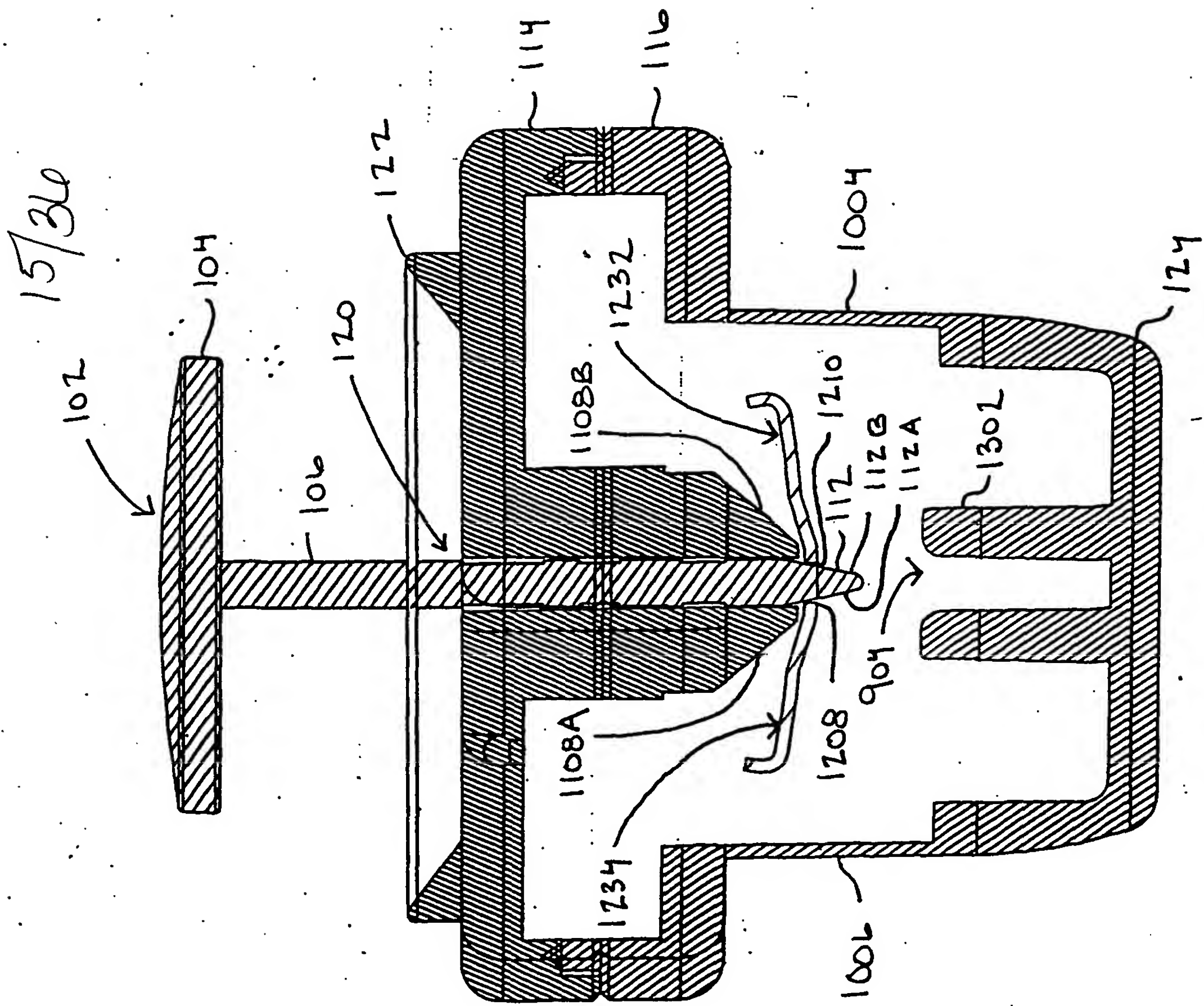


FIG. 15

Fig. 16

101
∴



Fig. 17

Fig. 18

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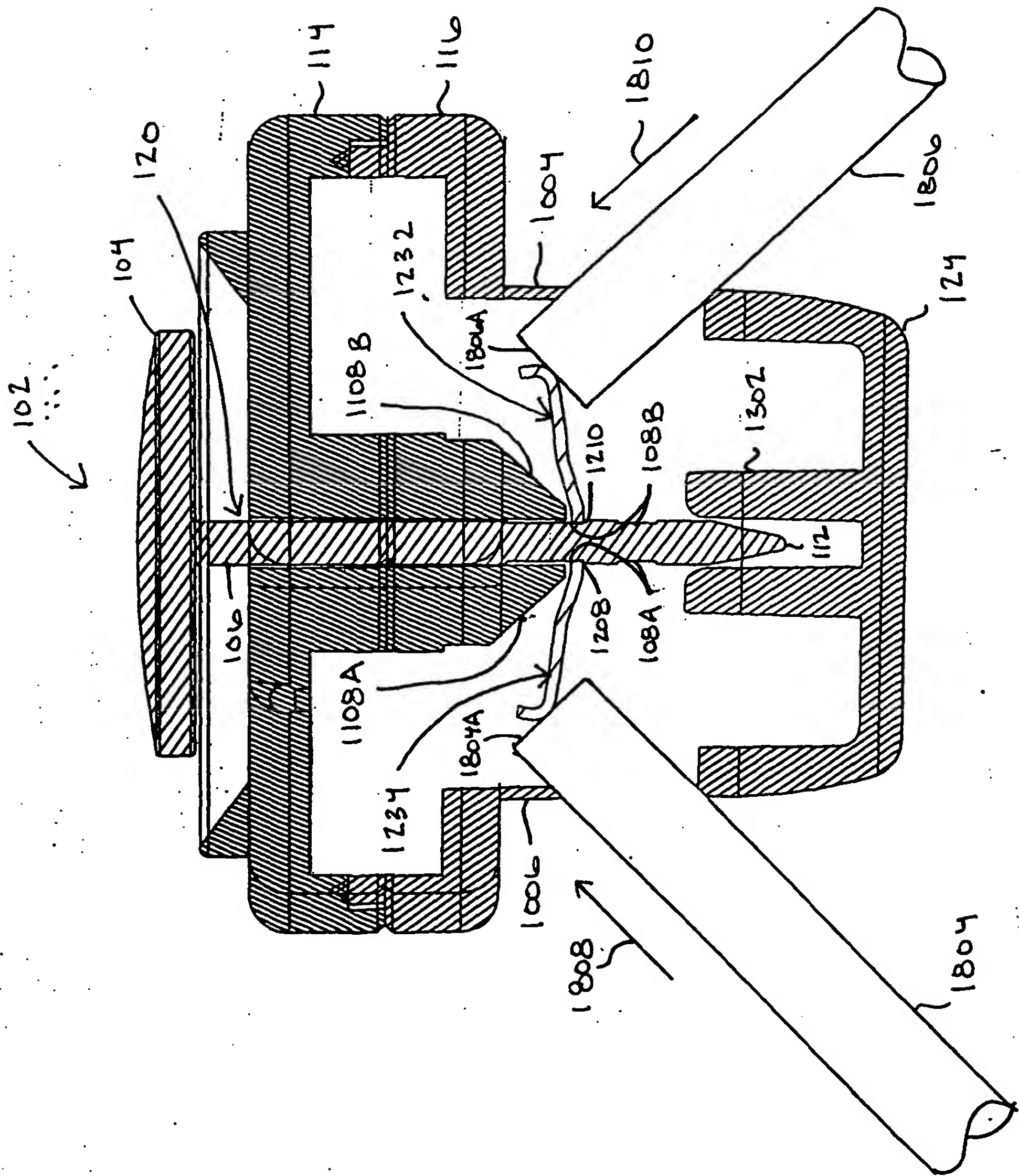


FIG. 19

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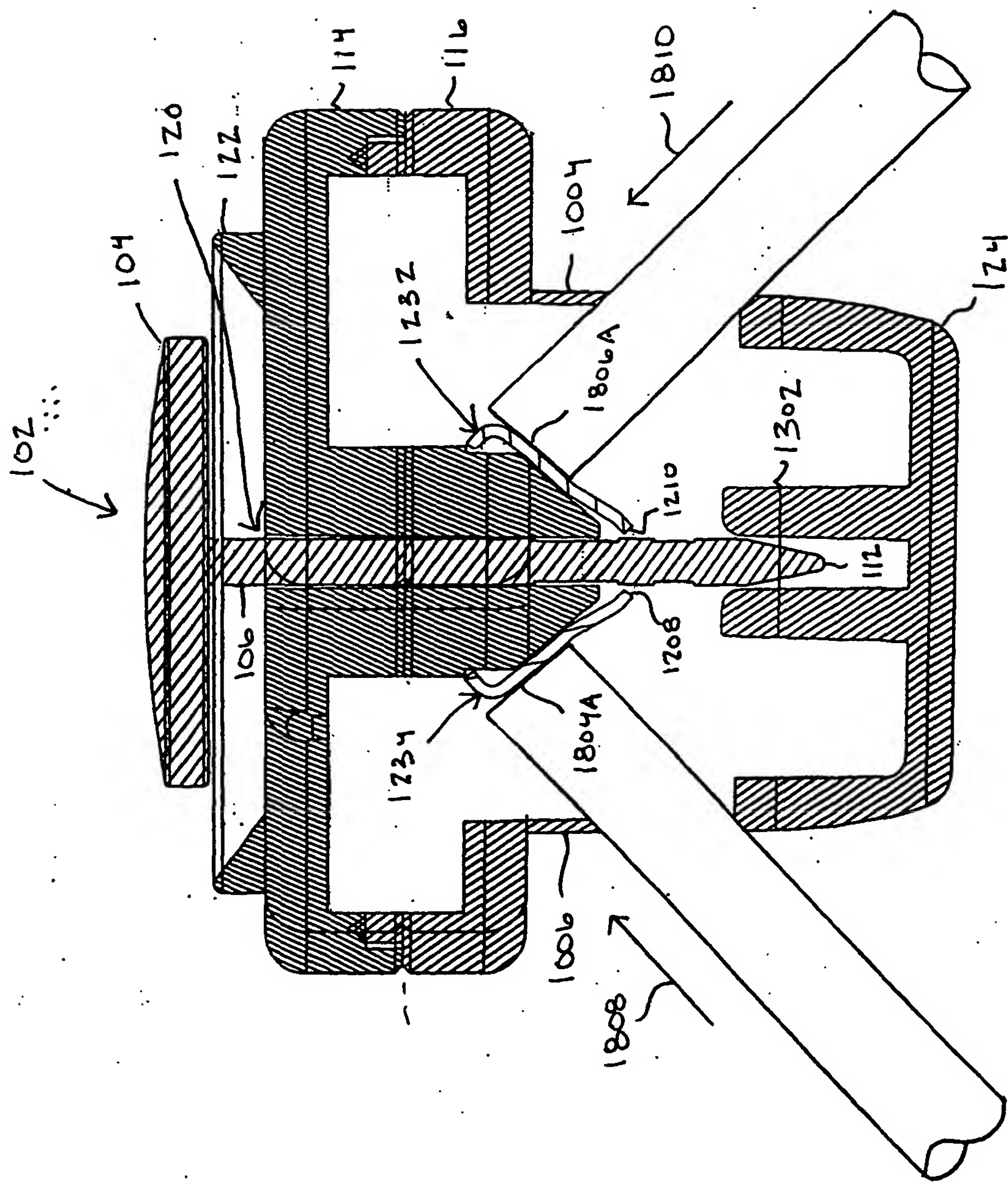


FIG. 20

[illegible]

Fig. 21

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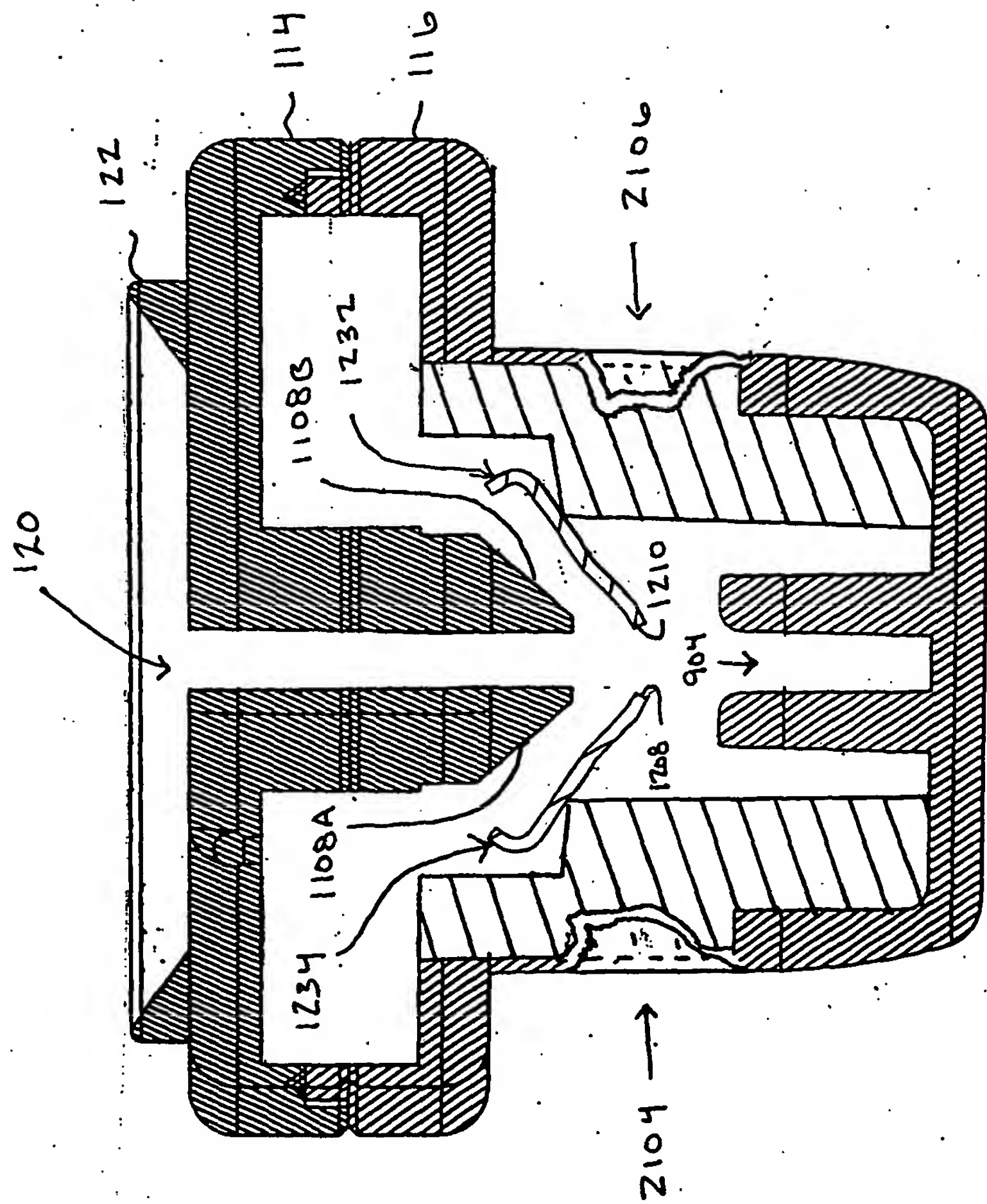


FIG. 22

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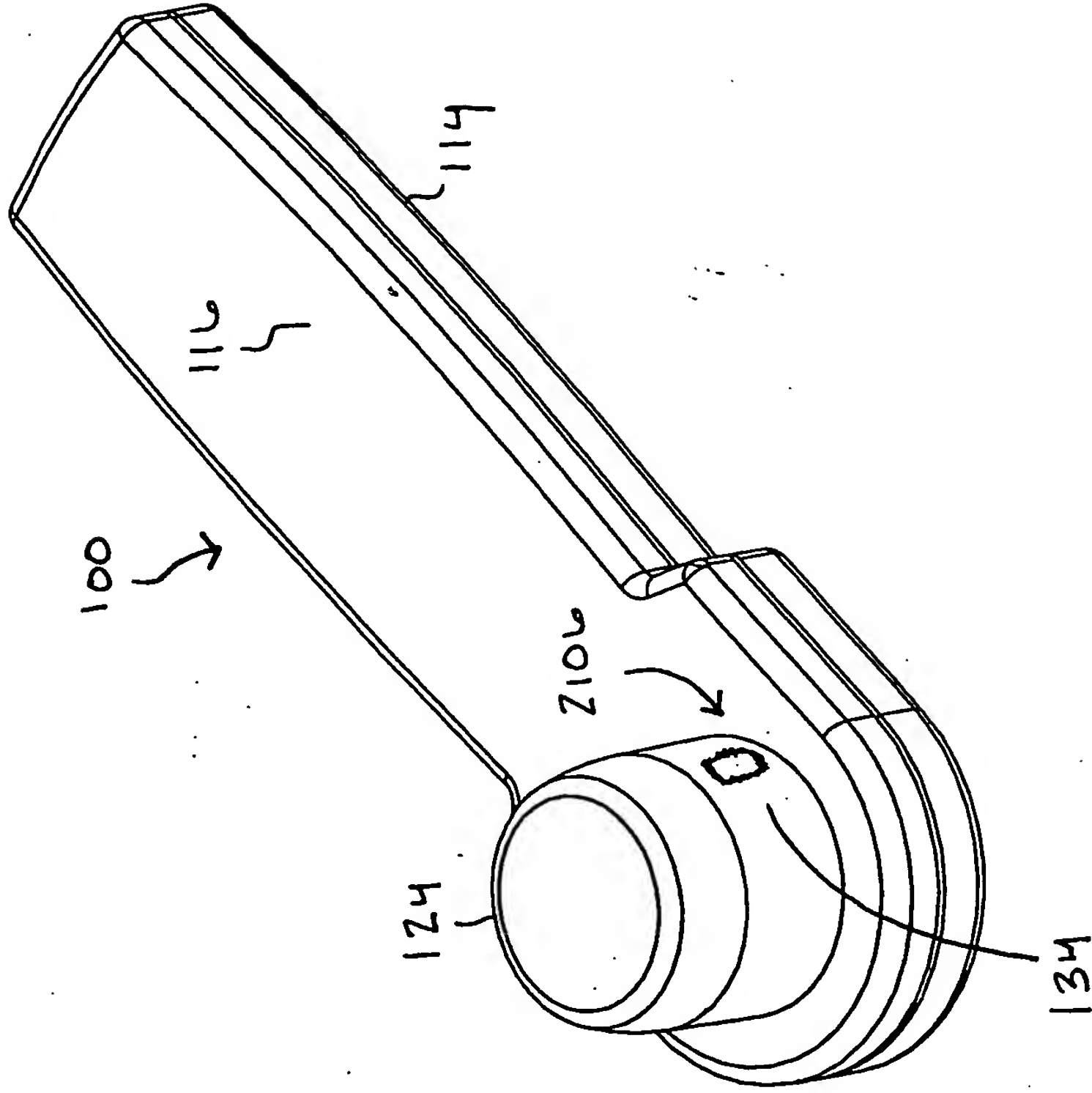
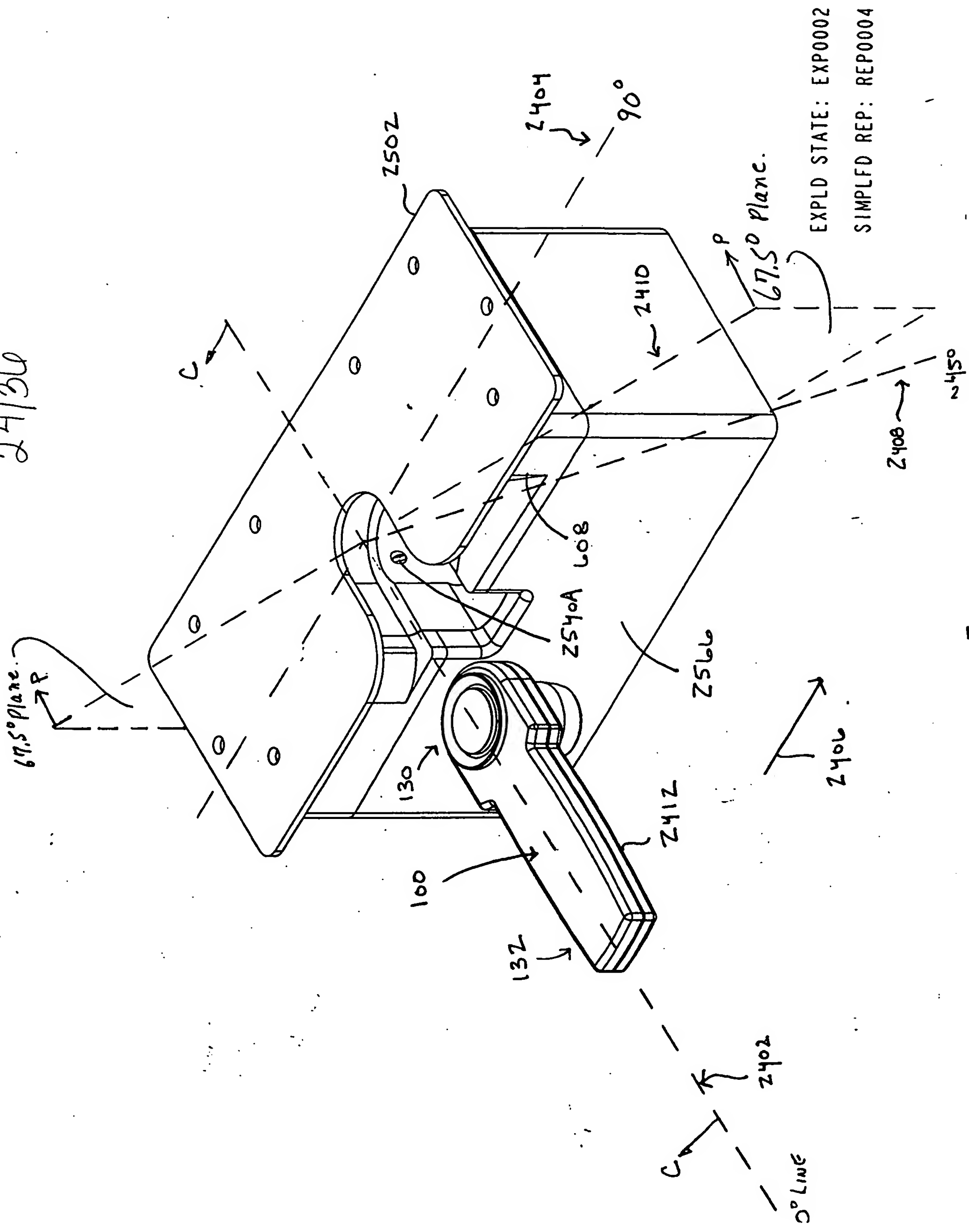


FIG. 23

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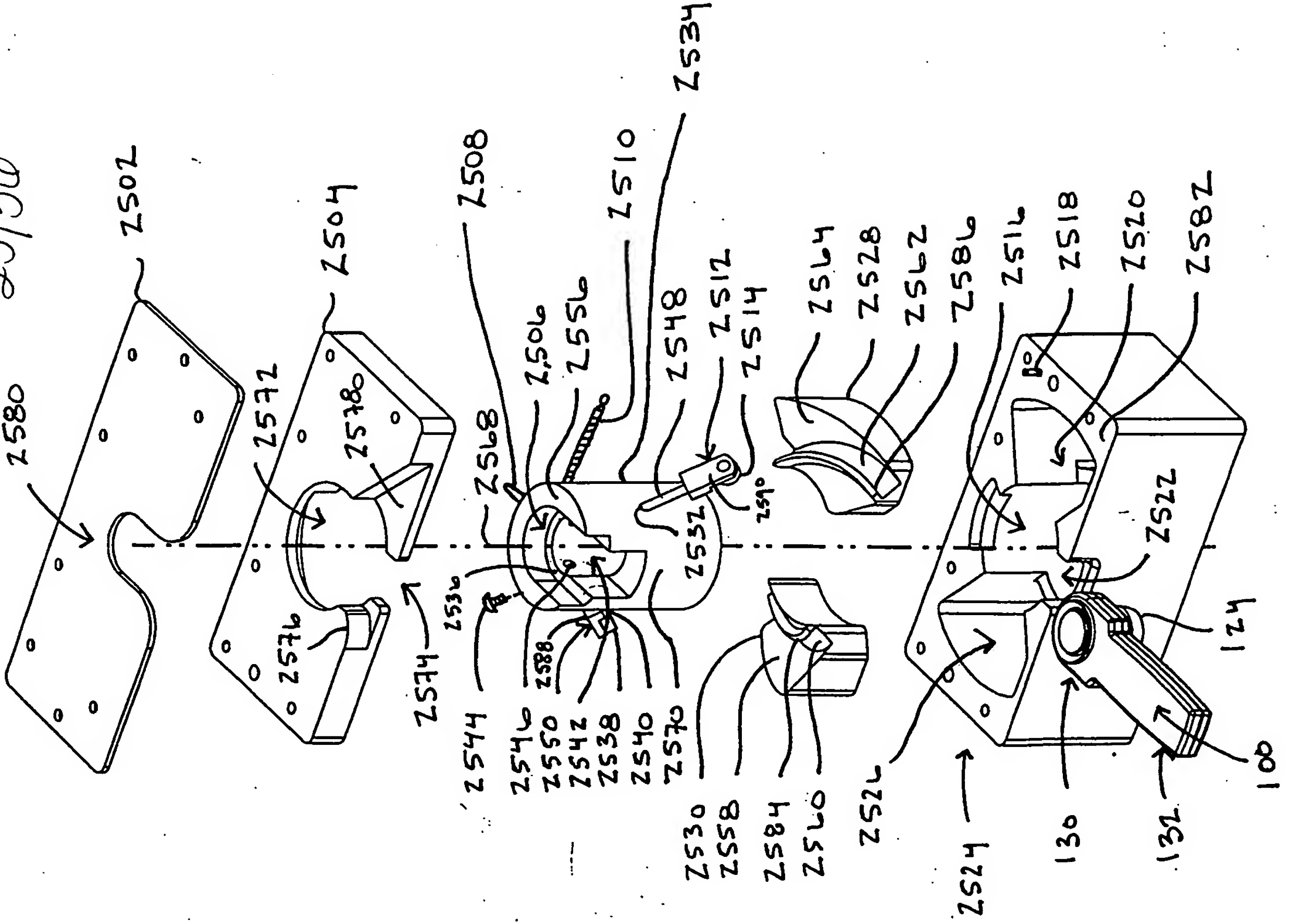


EXPLD STATE: EXP0002
SIMPLFD REP: REP0004

FIG. 24

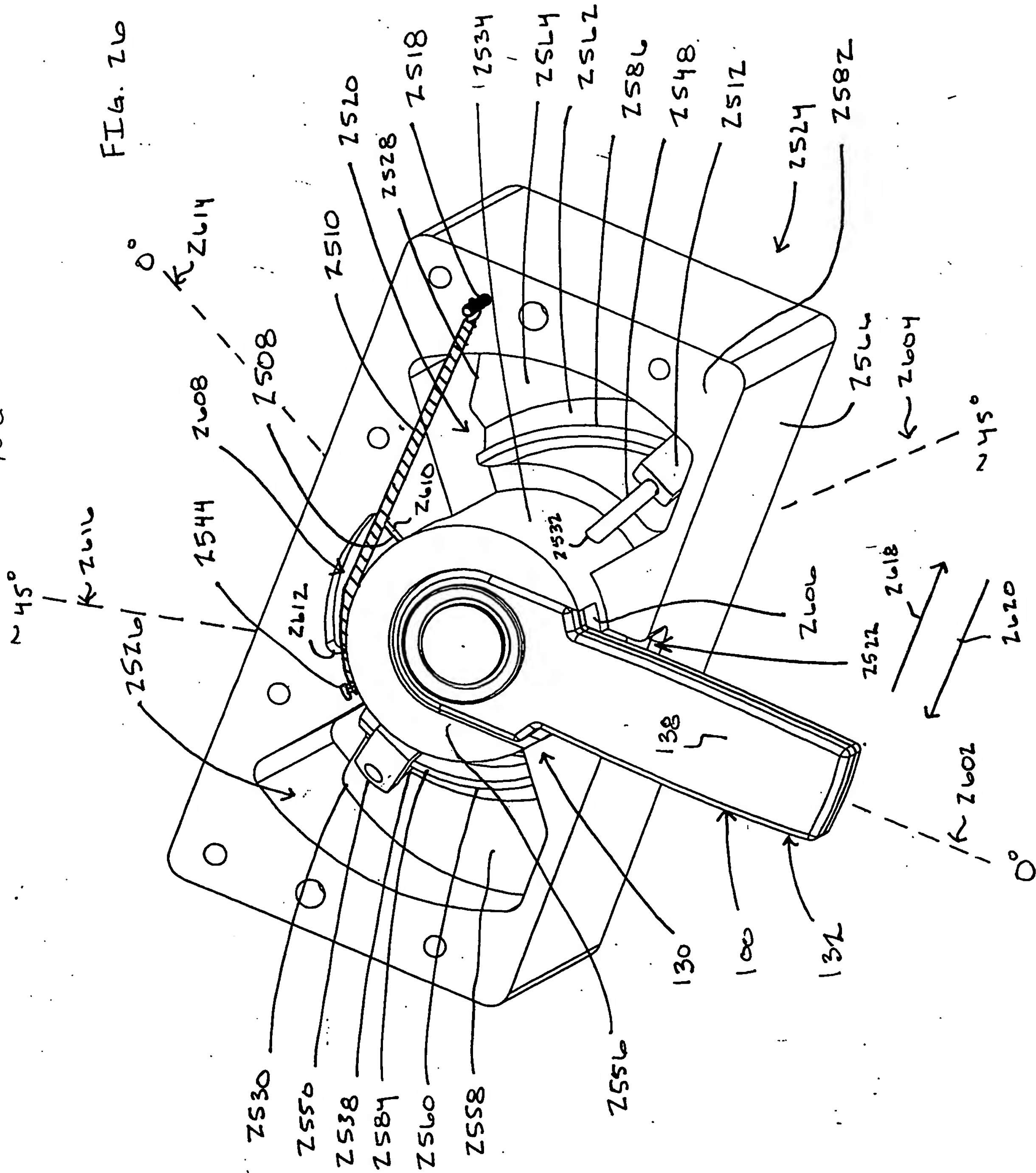
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FIG. 25



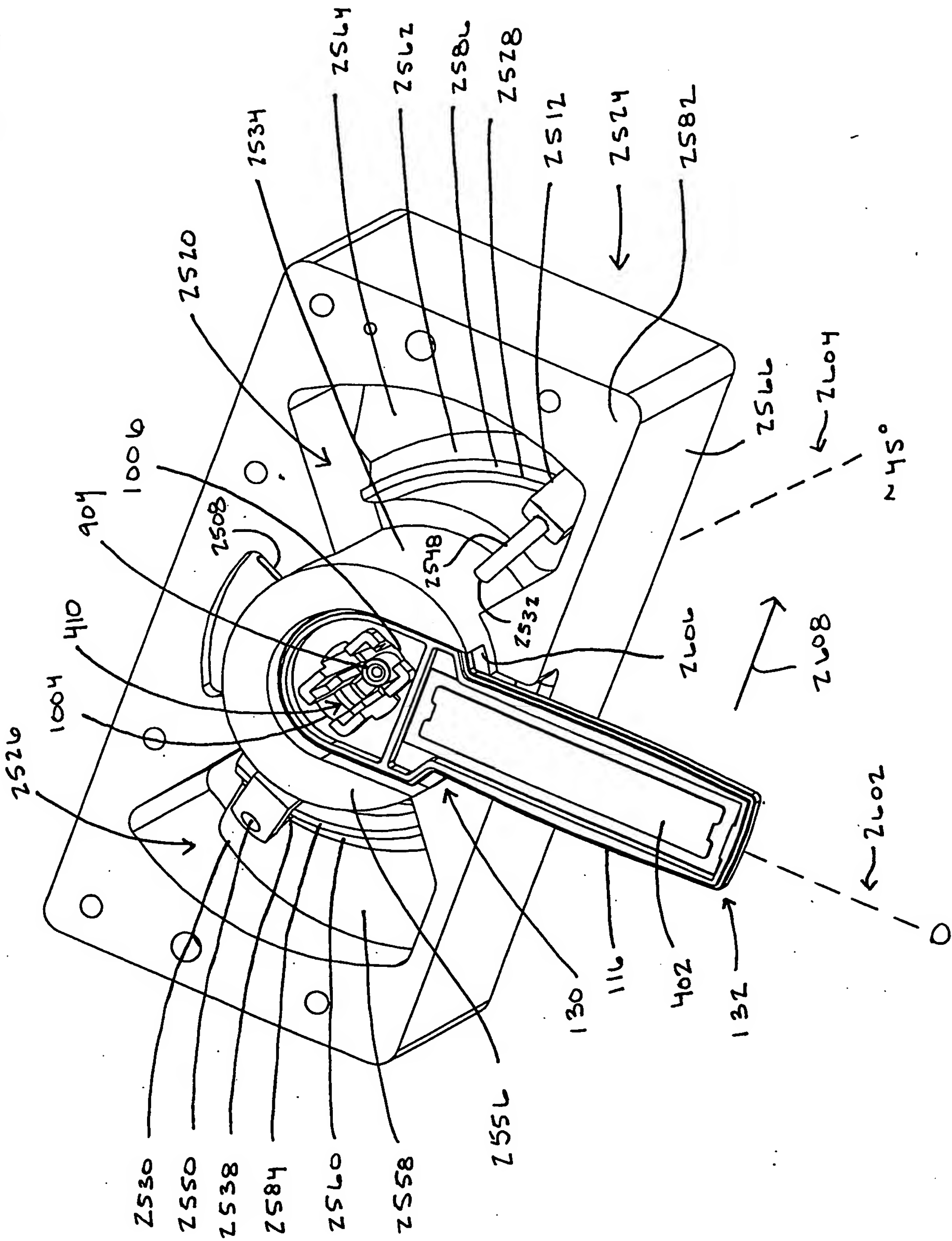
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FIG. 26



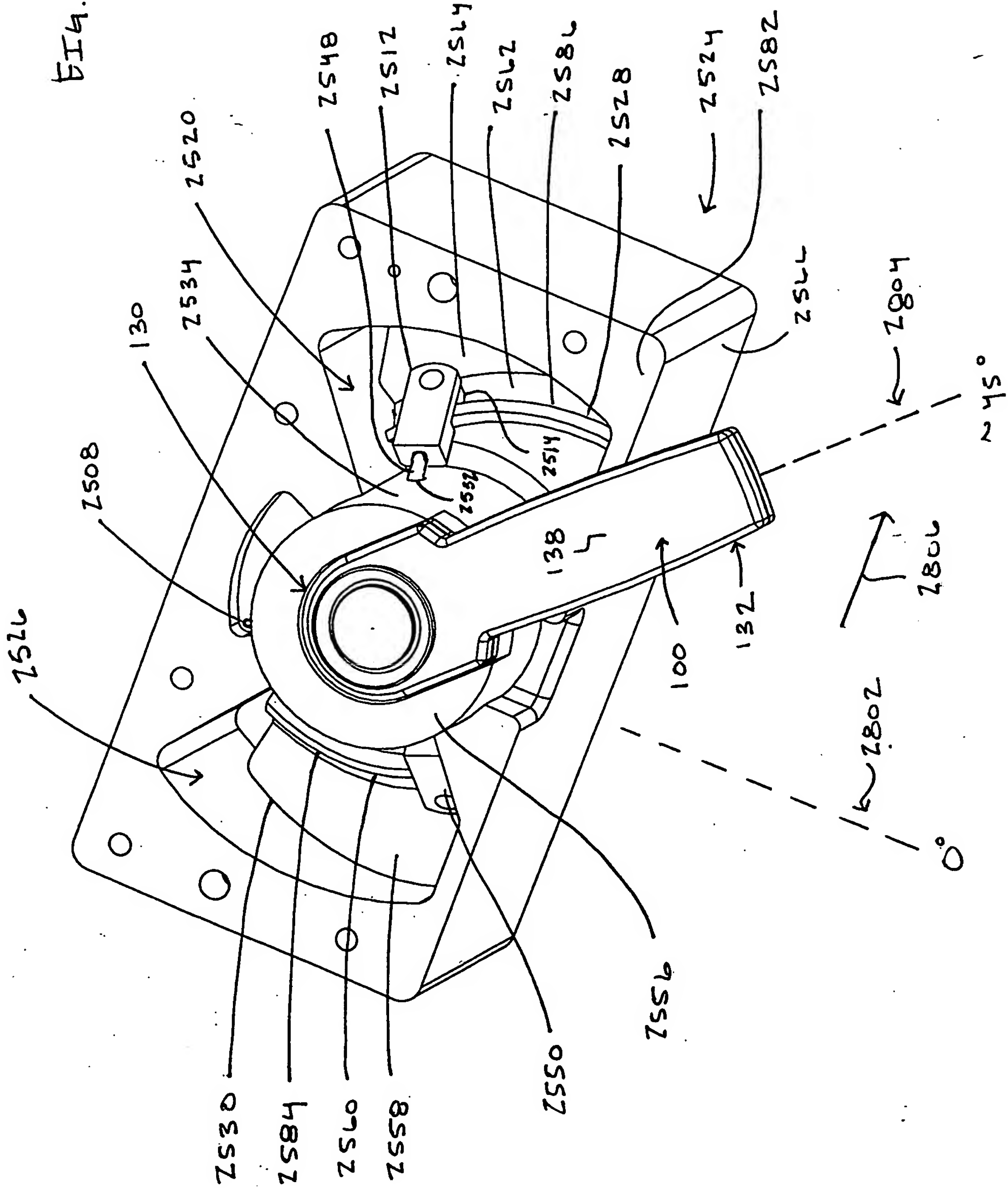
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FIG. 27



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FIG. 28



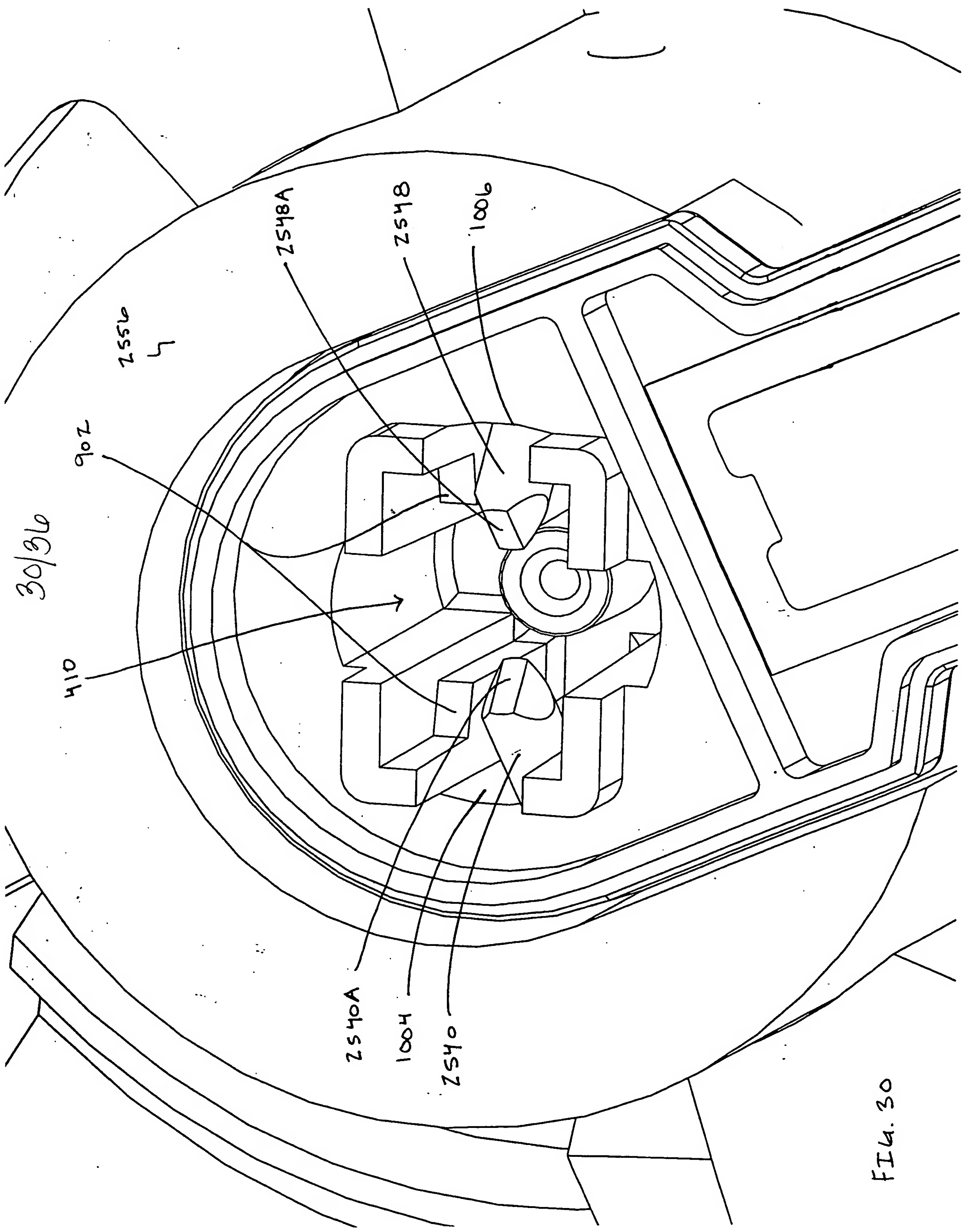


FIG. 30

FI 4.31

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3100

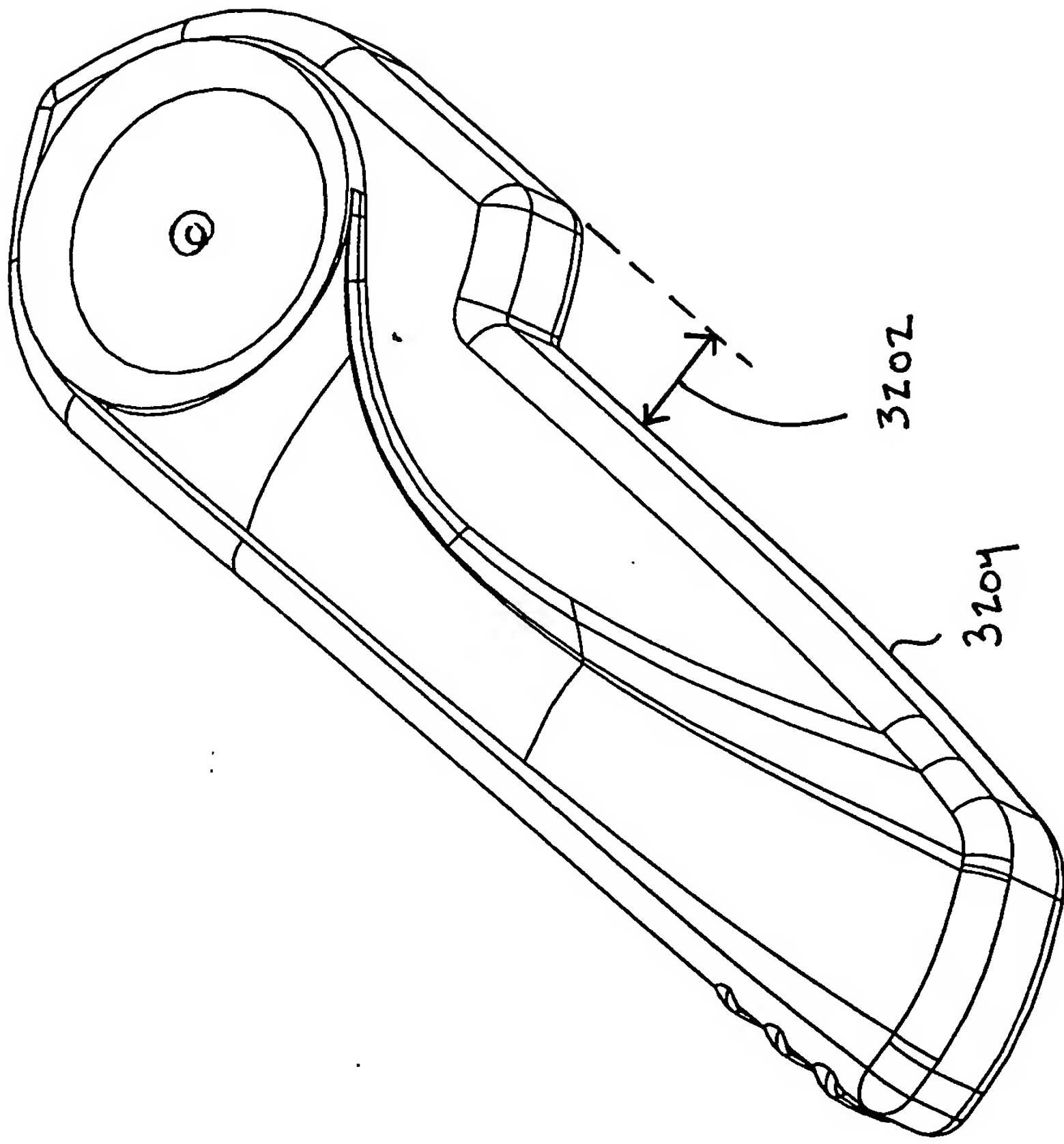


FIG. 32

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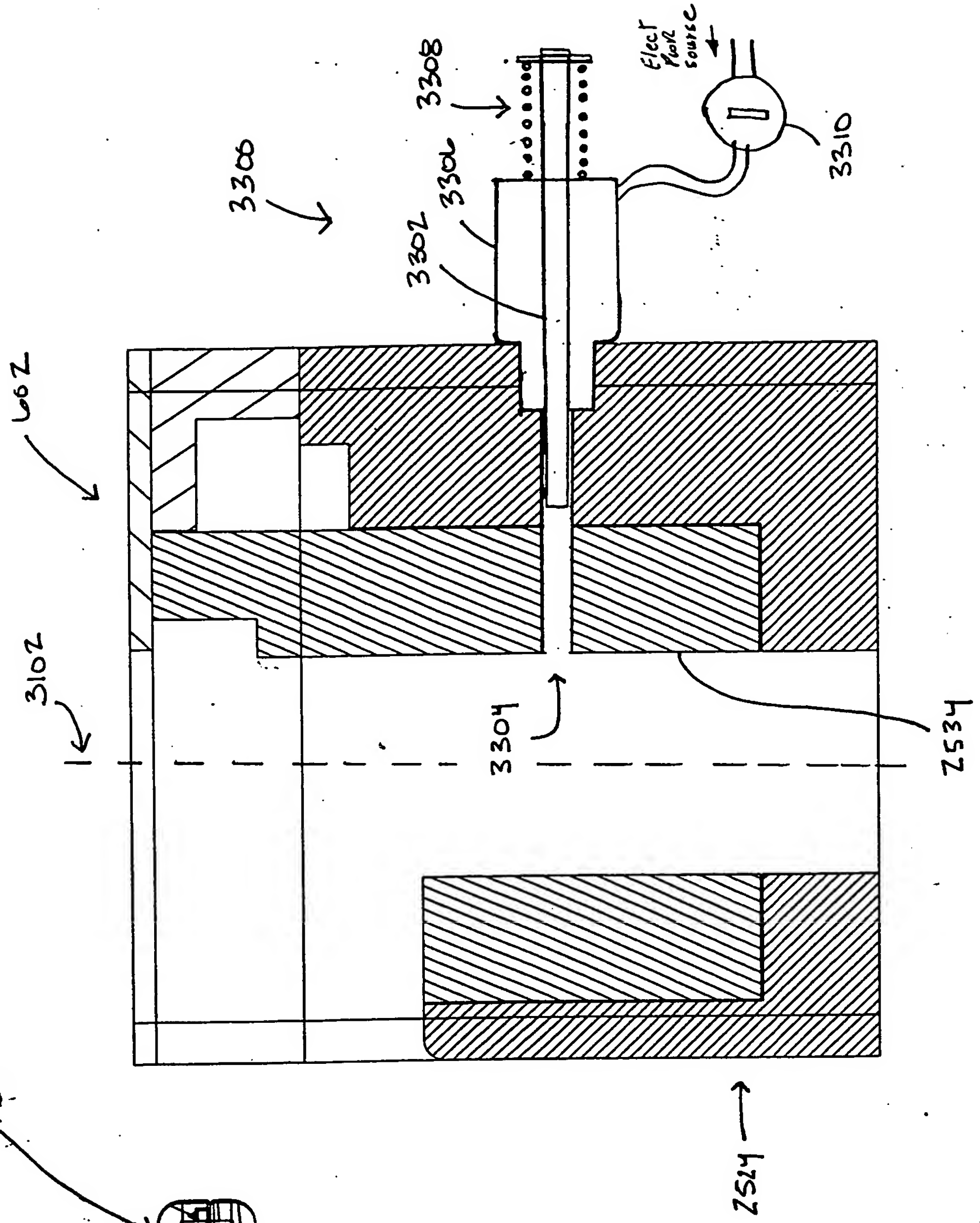
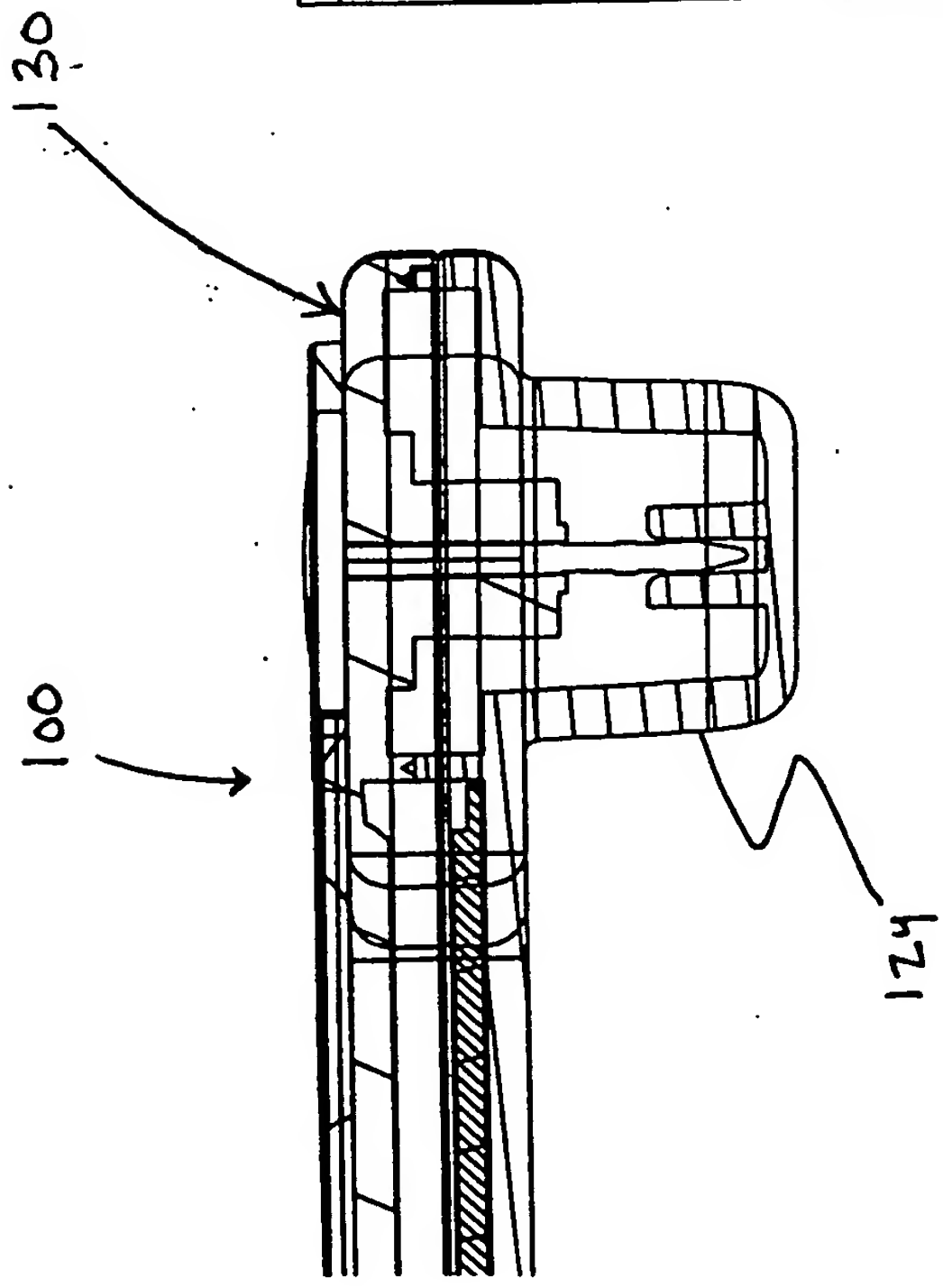


FIG. 33

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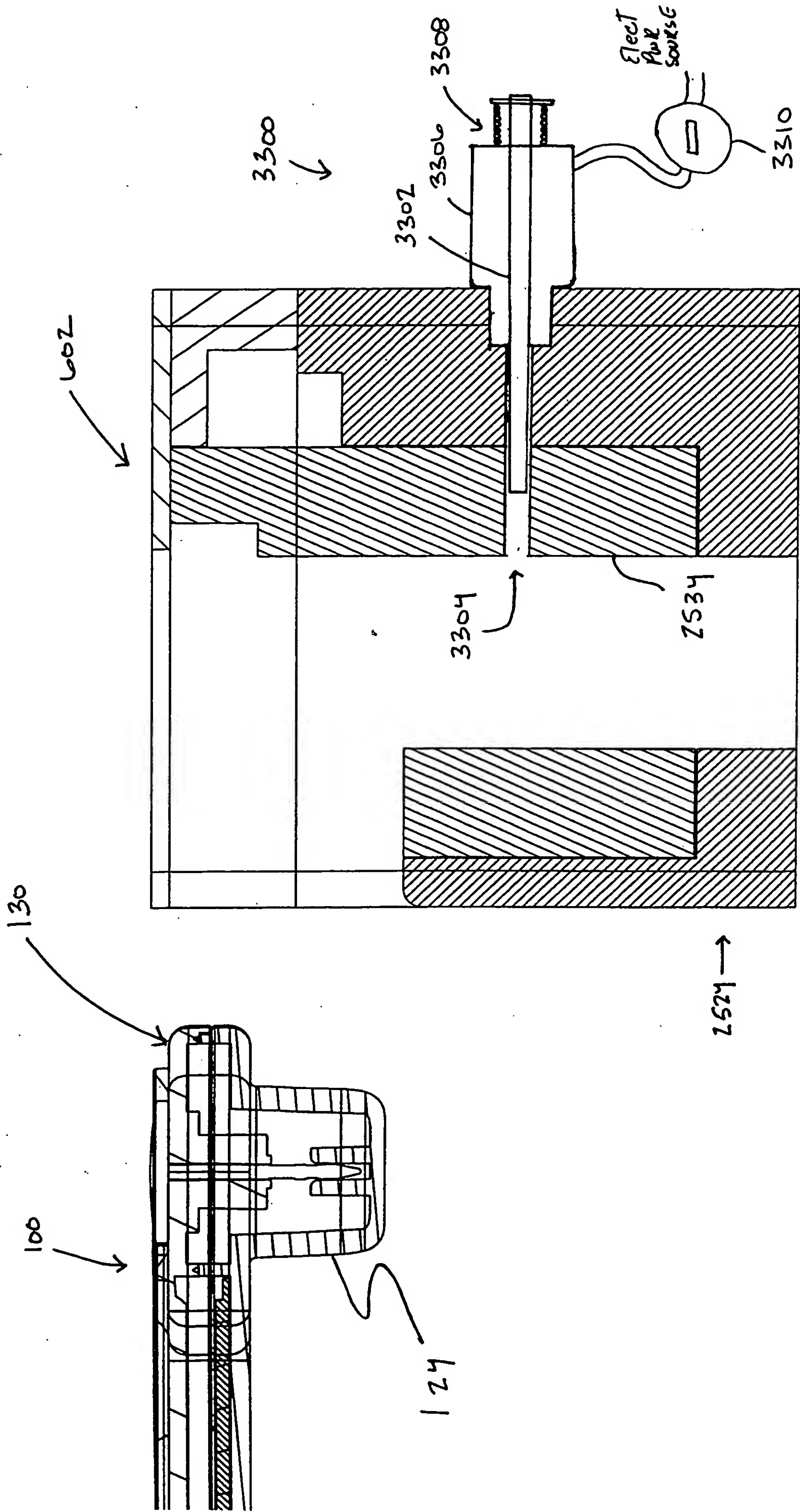


FIG. 34

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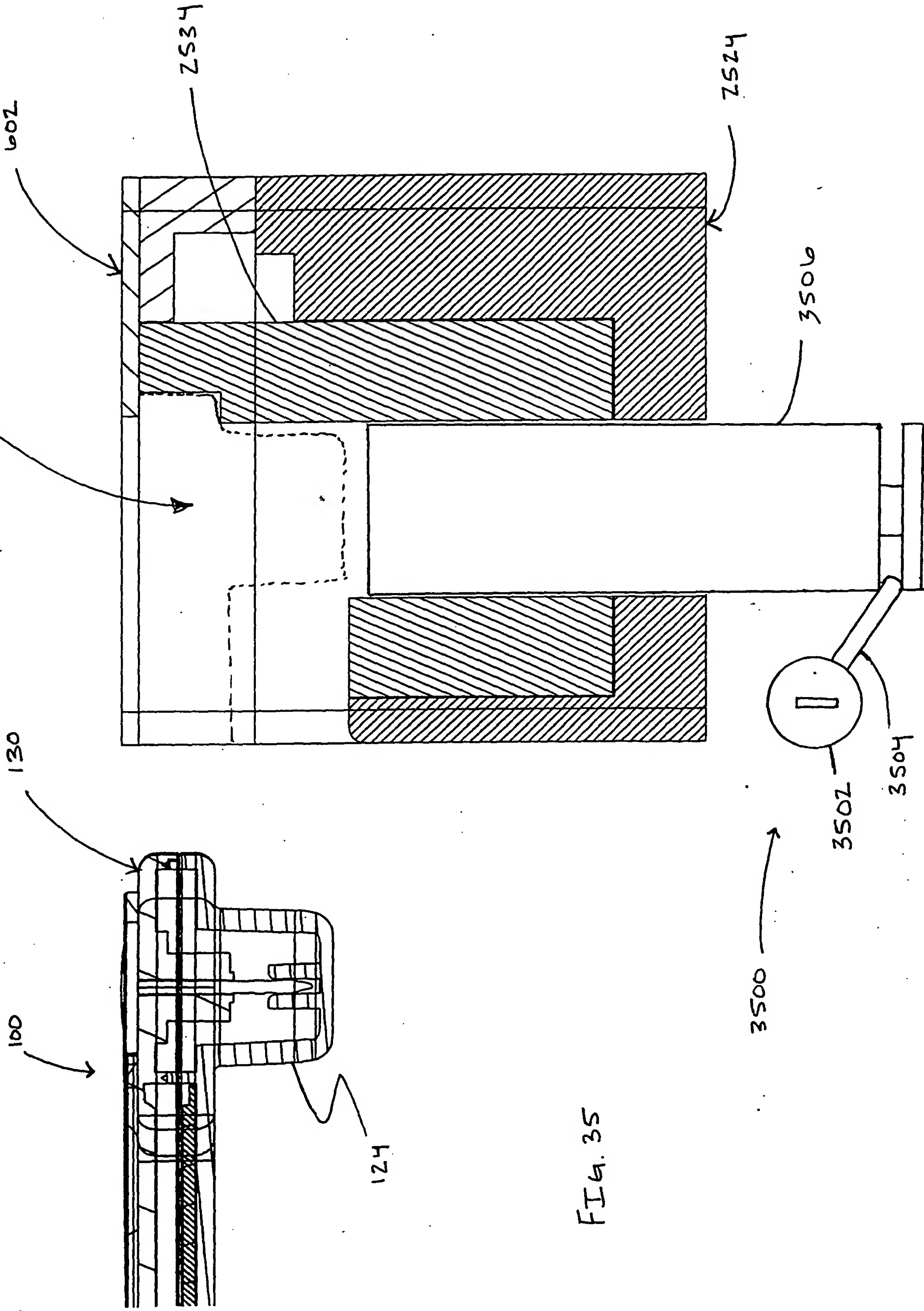


FIG. 35

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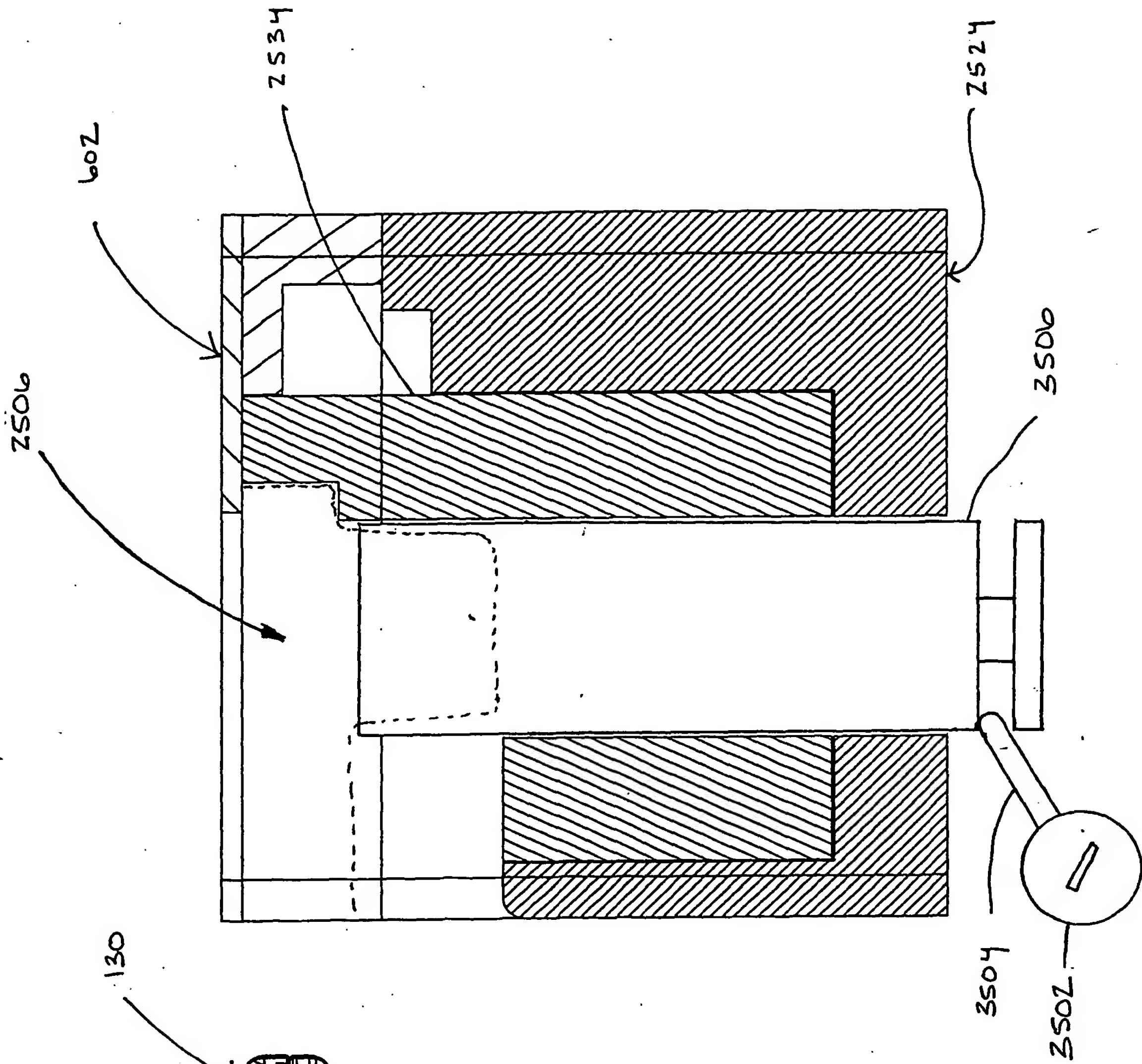
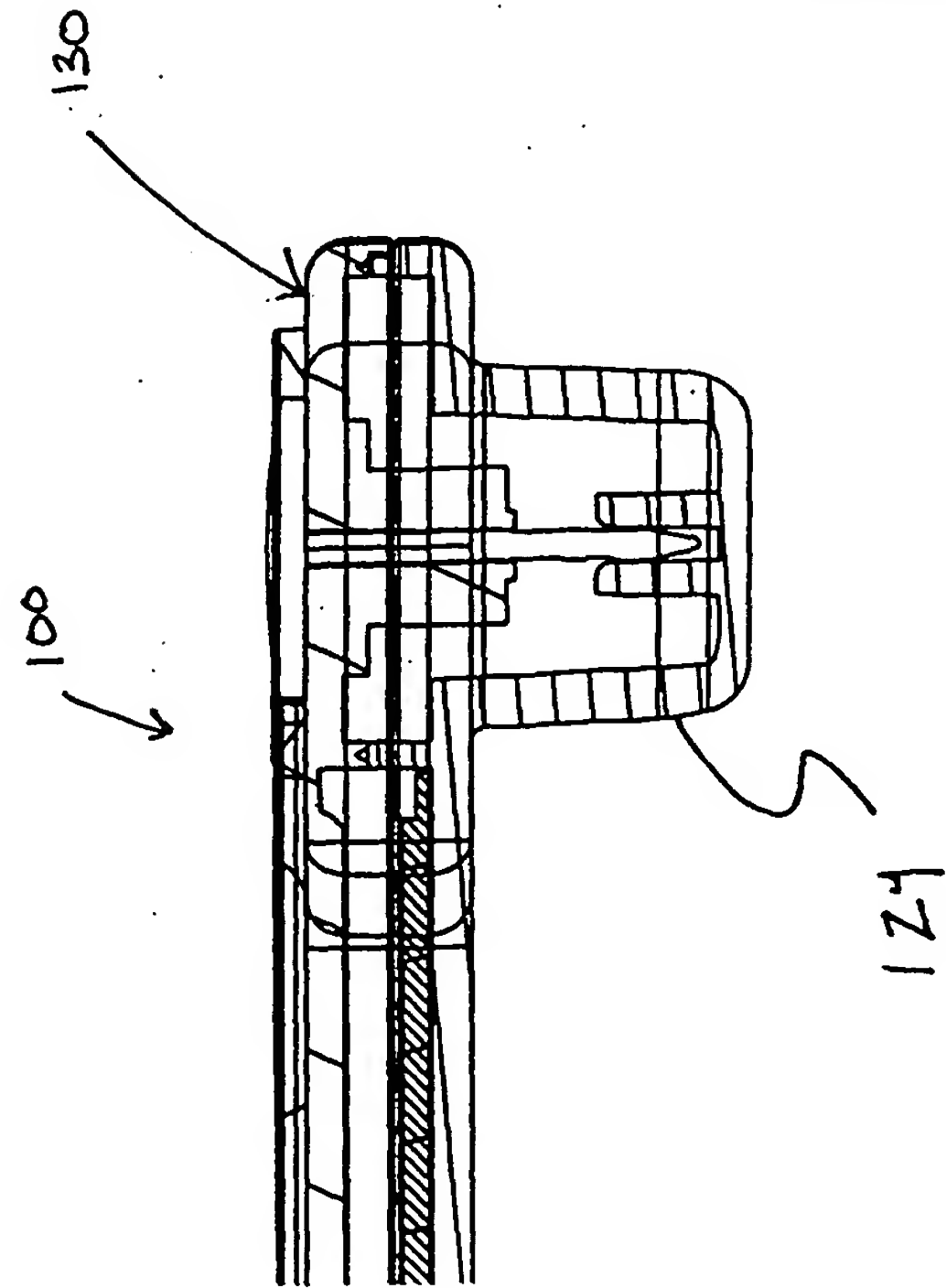


FIG. 36